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Analytical threshold voltage and drain-induced barrier lowering models of elliptic junctionless Gate-All-Around FET

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Abstract. The analytical models have been presented to determine the threshold voltage and Drain-Induced Barrier Lowering (DIBL) of an elliptic junctionless Gate-All-Around (GAA) FET. The values obtained using the proposed models were confirmed to be in good agreement, compared to other papers verified. Using this analytical threshold voltage and DIBL models, the threshold voltage and DIBL were analyzed according to the eccentricity of the elliptic cross-section structure. As a result, it was found that the absolute value of the minimum central potential increases as eccentricity increases, thereby increasing the threshold voltage. Additionally, the absolute value of the minimum central potential decreases as the drain voltage increases, thereby decreasing the threshold voltage, and this decreasing rate, i.e. DIBL, reduces as eccentricity increases. The threshold voltage and DIBL showed little change when the eccentricity was less than about 0.75, but a large change when it was more than 0.75. It was observed that the variation of the channel length and channel radius of the elliptic GAA FET had a significant effect on the rate of change of DIBL for eccentricity.

Keywords: Elliptic, Gate-All-Around, Threshold voltage, DIBL, Eccentricity.

Classification numbers: 2.2.2, 2.4.1, 4.1.1.

1. INTRODUCTION

The power dissipation and low voltage requirements have become important factors in increasingly smaller transistors to improve integration. To meet these demands, research is being conducted on transistor structures to improve carrier control ability within the channel by gate voltage. In the meantime, increasing the area of the gate terminal surrounding the channel such as double-gate MOSFET, tri-gate FinFET, and gate-all-around (GAA) FET, many studies have been conducted to reduce the short channel effects (SCEs) such as FET with high-*k* as gate oxide or negative capacitance FET using ferroelectric [1 - 5]. Among these, the structure that has recently attracted the most attention is the GAA FET, in which the entire gate is surrounded by metal [6 - 10]. Research on GAA FET is increasing day by day due to its advantage of being able to control carriers within the channel more effectively than FinFET. Accordingly, various types of GAA FET have been studied [11 - 13]. However, the SCEs such as degradation of subthreshold swing and on-off current ratio as the channel length becomes smaller appear to be

unavoidable problems. In particular, a constant and low threshold voltage is essential for stable operation and low power dissipation of the transistor [14].

It is difficult to manufacture ideal circular GAA structures due to the irregular directionality of oxidation that occurs during the etching and deposition processes that are essential in the production of GAA structures [15 - 16]. Research on the elliptic GAA FET fabricated at this time has been conducted [17 - 19]. However, not much research on elliptic GAA FETs has been found recently, as the research was mainly conducted about 10 years ago. Therefore, we present an analytical model for threshold voltage and drain-induced barrier lowering (DIBL) for GAA FET with an elliptic structure, prove its validity, and use this model to analyze SCEs of an elliptic GAA FET. In the meantime, several papers for the elliptic GAA FET used a potential distribution model to analyze the circular GAA FET by calculating the effective radius R_{eff} of the circular GAA FET corresponding to the elliptic structure [20]. Additionally, the analysis was focused on the aspect ratio (AR), which is the ratio of the major and minor axis lengths of the elliptic cross-section [21 - 22]. In other words, the SCEs for changes in AR were analyzed by fixing the length of the major axis or minor axis and changing the length of the remaining axis. However, if the AR changes, the SCEs will naturally change. As the AR increases, the size of the elliptic cross section will eventually increase, resulting in a change in SCEs. The changes in SCEs can be compared according to the AR only if the areas of the circular cross-section and the elliptic cross-section are the same. Therefore, in this paper, the SCEs such as threshold voltage and DIBL were analyzed for circular GAA FET and elliptic GAA FET with the same cross-sectional area.

Recently, Chiang [23] presented the threshold voltage of the junction-based NMOS and PMOS elliptic FET. Kumar *et al.* [24] observed the change in g_m/I_{ds} according to the change in minor diameter in the case of elliptic FET, and the change in threshold voltage according to the elliptic cross-section can be predicted from Kumar's results. Threshold voltage and DIBL are related to gate and drain voltage. In other words, those will interfere with the stable operation if those change depending on the applied voltage, so it must be sufficiently predictable, based on device parameters. Therefore, we will present an analytical model for threshold voltage and DIBL analysis of the elliptic structure that is indispensably manufactured. In particular, we will analyze the junctionless FETs rather than the junction-based FETs, which have processing difficulties in short channels. The junctionless FET has been studied extensively since Colinge *et al.* [25 - 26] proposed. We will present an analytical threshold voltage and DIBL models of an elliptic GAA FET with a junctionless structure.

2. THRESHOLD VOLTAGE AND DIBL OF ELLIPTIC JUNCTIONLESS GAA FET

2.1. Structure of elliptic junctionless GAA FET

Figure 1 shows the cross-sectional structures of the circular GAA FET and the elliptic GAA FET when AR = 1.2, 1.5, and 2. The x-axis is the major axis, the y-axis is the minor axis, and the direction perpendicular to the paper surface is the z-axis, that is, the channel length direction. As shown in Fig. 1, the threshold voltage and DIBL will be analyzed for the aspect ratio AR = a/b when the channel cross-sectional area (πR^2) of the circular GAA FET and the channel cross-sectional area (πab) of the elliptic GAA FET with the length a of the major axis and the length b of the minor axis are the same, that is, in the case of $R^2 = ab$. The channel material is silicon, and the gate oxide film is SiO_2. The doping concentration of the channel is $10^{19}/cm^3$. The device parameters used in this paper are listed in Table 1.

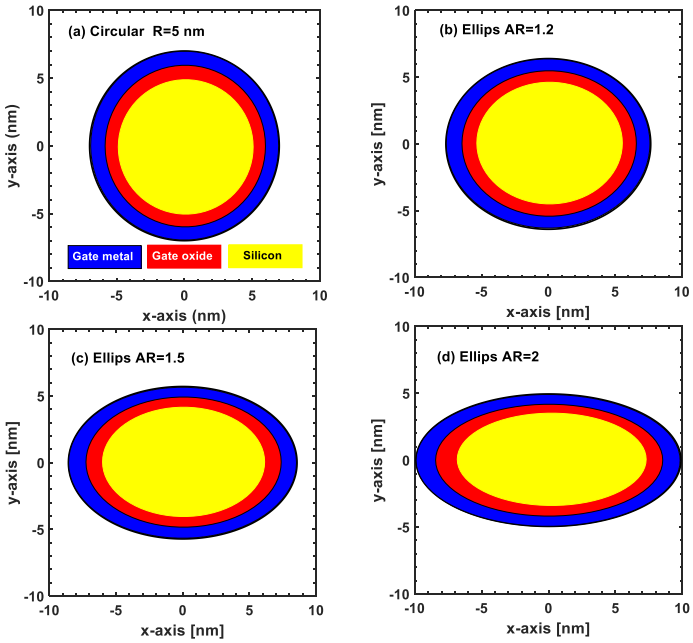

Figure 1. Cross-sectional view of (a) circular and elliptic junctionless GAA FET at (b) AR = 1.2, (c) AR = 1.5, and (d) AR = 2.

Table 1. Device parameters for this analytical SS model.

Device parameter	Symbol	Value
Channel length	L_g	10~60 nm
Channel radius	R	5 nm
Oxide thickness	t_{ox}	2 nm
Doping concentration	N_d	10^{19} /cm^3
Eccentricity	e	0 ~ 0.99

The eccentricity e of an ellipse can be expressed as Eq. (1).

$$e = \sqrt{1-\left(\frac{b}{a}\right)^2} = \sqrt{1-\left(\frac{1}{AR}\right)^2} \tag{1}$$

where

$$AR = 1/\sqrt{1-e^2}\ ,\ R^2 = ab\ ,\ b = R/\sqrt{AR}\ ,\ a = b\times AR\ .$$

In the case of a junctionless FET, most carriers move along the central axis of the channel, so potential distribution in the center of the channel is ultimately required. In this paper, Chaing's central potential model for a junction-based FET was modified to obtain the potential distribution in the center of the channel for a junctionless FET as Eq. (2) [23].

$$\frac{d^2\phi_C(z)}{dz^2} + \frac{\phi_C(z)-\varphi_{CL}}{\lambda^2} = 0 \tag{2}$$

where

$$\varphi_{CL} = V_{gs} - V_{fb} + \frac{qN_d\lambda^2}{\varepsilon_{si}} \ .$$

Here, $\phi_c(z)$ is the potential of the central axis obtained along the channel direction of the *z*-axis as in Eq. (3). The φ_{CL} represents the long channel central potential, the λ and V_{fb} represent the scaling length and the flat-band voltage, respectively. The scaling length λ is as in Eq. (3).

$$\frac{1}{\lambda^2} = \frac{1}{\lambda_a^2} + \frac{1}{\lambda_b^2} = \frac{2C_{ox}}{2a\varepsilon_{si} + C_{ox}a^2} + \frac{2C_{ox}}{2b\varepsilon_{si} + C_{ox}b^2} \tag{3}$$

Here, C_{ox} is the effective capacitance per unit area of the gate oxide film [23], and ε_{ox} and ε_{si} represent the dielectric constants of SiO_2 and Si, respectively. As shown in Eq. (2) and Eq. (3), to obtain the central potential distribution, not only the material parameters are needed, but also the values of the lengths *a* and *b* of the major and minor axes and the effective radius R_{eff}. In Eq. (3), the R_{eff} is the effective radius assuming that the ellipse is a circle, and can be obtained from Eq. (4) as follows [22]:

$$\frac{4\varepsilon_{ox}}{2\varepsilon_{si}R_{eff}t_{ox} + \varepsilon_{ox}R_{eff}^2} = \frac{2\varepsilon_{ox}}{2\varepsilon_{si}at_{ox} + \varepsilon_{ox}a^2} + \frac{2\varepsilon_{ox}}{2\varepsilon_{si}bt_{ox} + \varepsilon_{ox}b^2} \tag{4}$$

Many papers used approximation equations according to the sizes of *a*, *b*, and t_{ox}, but in this paper, the exact R_{eff} of Eq. (4) was obtained using MATLAB's *solve* command.

2.2. Analytical threshold voltage model for elliptic junctionless GAA FET

In this paper, the threshold voltage defined by Hu *et al.* [27] was used. That is, the threshold voltage was defined as the gate voltage when the difference between the minimum voltage in the channel and the reference voltage is twice the thermal voltage V_t, and this is considered reasonable for a fully depleted channel where mobile charges can be ignored. Based on this definition, the minimum central potential can be obtained from Eq. (2) according to Chaing's expansion method [23] as follows:

$$\phi_{C\min}(z = z_{\min}) = 2\sqrt{AB} + \varphi_{CL} \tag{5}$$

where

$$z_{\min} = \frac{\lambda}{2}\ln\left(\frac{A}{B}\right)$$

$$A = \frac{\left(V_{bi} - \varphi_{CL}\right)\left(e^{\frac{L_g}{\lambda}} - 1\right) - V_{ds}}{2\sinh\left(\frac{L_g}{\lambda}\right)} = \alpha V_{gs} + \beta,\ B = \frac{V_{ds} - \left(V_{bi} - \varphi_{CL}\right)\left(e^{-\frac{L_g}{\lambda}} - 1\right)}{2\sinh\left(\frac{L_g}{\lambda}\right)} = \gamma V_{gs} + \theta.$$

Therefore, the threshold voltage was obtained by finding the gate voltage that satisfies the following Eq. (6):

$$\phi_{C\min}(z = z_{\min}) = 2\sqrt{AB} + \varphi_{CL} = V_{bi} - 2V_t \tag{6}$$

Here, V_{bi} is the reference voltage as the junction potential between the source and channel, and V_t is the thermal voltage *kT/q* defined by the Boltzmann constant *k* and the absolute temperature *T*. Expressing Eq. (6) in terms of the value of V_{gs}, it becomes the following Eq. (7).

$$2\sqrt{(\alpha V_{gs}+\beta)(\gamma V_{gs}+\theta)}+V_{gs}-V_{fb}+\frac{qN_D\lambda^2}{\varepsilon_{si}}=V_{bi}-2V_t \tag{7}$$

The root of Eq. (7) can be obtained as following Eq. (8), and this root can be called the threshold voltage.

$$V_{th}=\frac{-B_1+\sqrt{B_1^2-4A_1C_1}}{2A_1} \tag{8}$$

where

$$A_1=(4\alpha\gamma-1),\ B_1=\left[4(\alpha\theta+\beta\gamma)+2\left(V_{fb}-\frac{qN_D\lambda^2}{\varepsilon_{si}}+V_{bi}-2V_t\right)\right],\ C_1=4\beta\theta-\left(V_{fb}-\frac{qN_D\lambda^2}{\varepsilon_{si}}+V_{bi}-2V_t\right)^2.$$

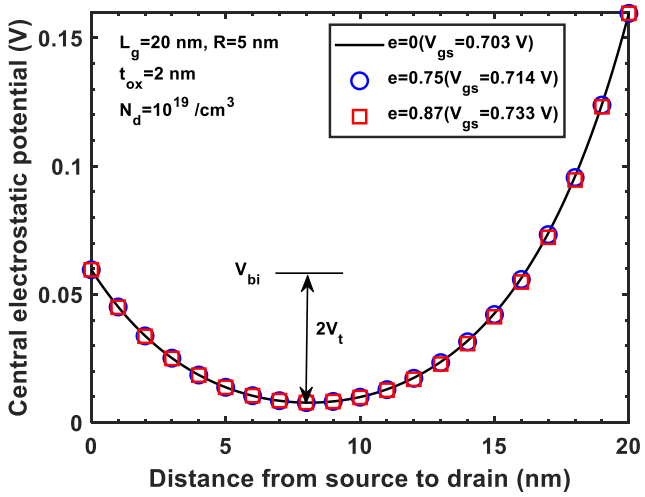

Figure 2. Central electrostatic potentials with the eccentricity as a parameter to obtain the threshold voltage under the given conditions in the figure.

Figure 2 shows the central electrostatic potential distributions corresponding to the gate voltages when the minimum central potential becomes V_{bi}-$2V_t$ in the case the eccentricity is 0, 0.75, and 0.87, respectively, under the given conditions. The gate voltage according to the eccentricity indicated in the legend ultimately becomes the threshold voltage.

2.3. Analytical DIBL model for elliptic junctionless GAA FET

The DIBL is defined as the change in threshold voltage according to the drain voltage as shown in the following Eq. (9).

$$DIBL=-\frac{dV_{th}}{dV_{ds}}=\frac{1}{2A_1}\frac{d}{dV_{ds}}\left(B_1-\sqrt{B_1^2-4A_1C_1}\right)=\frac{1}{2A_1}\left\{\frac{dB_1}{dV_{ds}}-\frac{B_1\frac{dB_1}{dV_{ds}}-2A_1\frac{dC_1}{dV_{ds}}}{\sqrt{B_1^2-4A_1C_1}}\right\} \tag{9}$$

The DIBL obtained by Eq. (9) is shown in Fig. 3. As shown in Fig. 3, it can be observed that the DIBL value changes depending on the drain voltage V_{ds}. In other words, not only the

threshold voltage but also DIBL changes depending on V_{ds}. In most papers, the threshold voltages at two specific V_{ds1} and V_{ds2} are obtained, and their difference is divided by the difference between V_{ds1} and V_{ds2} [28-29].

In this case, the DIBL will change depending on the V_{ds1} and V_{ds2} used. In this paper, the intermediate value of V_{ds2} and V_{ds1} in Eq. (9) was used when compared with other papers to obtain DIBL in this way. As shown in Fig. 3, the DIBL value is constant regardless of the drain voltage as the channel length increases. However, the dependence of DIBL on the drain voltage increases as the channel length becomes shorter. In particular, the dependence of DIBL on drain voltage further increased when the drain voltage was low. This is considered to be a matter of caution when designing because it can cause problems with the stability of the logic circuit.

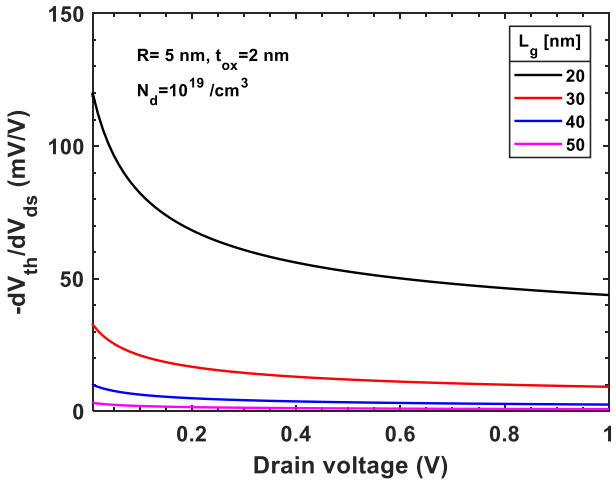

Figure 3. DIBLs for drain voltage with channel length as a parameter under the given conditions in the figure.

3. VERIFICATIONS AND RESULTS OF ANALYTICAL THRESHOLD VOLTAGE AND DIBL MODELS

3.1 Verifications of analytical threshold voltage and DIBL models

To show the validity of the analytical threshold voltage and DIBL models for the elliptic junctionless GAA FET obtained in Eqs. (8) and (9), the results of Hu's paper [27] are compared in Figs. 4 and 5. As shown in Figs. 4 and 5, the analytical threshold voltage and DIBL models presented in this paper matched well with the results of Hu's papers. Therefore, we will analyze the elliptic junctionless GAA FET using the analytical threshold voltage and DIBL models derived in Section 2.2. and Section 2.3.

3.2 Analysis of threshold voltage and DIBL for elliptic GAA FET

To investigate the effect of the eccentricity on the threshold voltage, the effective radius and threshold voltage for the eccentricity were plotted using Eqs. (4) and (8). As shown in Fig. 6, the threshold voltage increases as eccentricity increases. This is believed to be due to a decrease in the effective radius shown in Fig. 6. To consider this in more detail, the minimum central potential distribution is shown in the inset of Fig. 6 using Eq. (5). As described above,

the threshold voltage increases as the absolute value of the minimum central potential increases. As shown in the inset of Fig. 6, the absolute value of the minimum central potential increases in the region of $e > 0.75$ due to the increase in eccentricity, and as a result, the threshold voltage suddenly increases in this region.

Minimum central potential directly affects the threshold voltage and will also change depending on the drain voltage. In Fig. 7, the change in central potential distribution at a channel length of 20 nm and a channel radius of 5 nm is shown according to changes in drain voltage and eccentricity. To enlarge the minimum potential area, only a portion of the central channel area is shown. As shown in Fig. 7, the minimum central potential increases as the drain voltage increases and the increase becomes smaller when the eccentricity is large. Due to this, it can be predicted that DIBL decreases when the eccentricity increases. In other words, the change in the minimum central potential according to the drain voltage will be equal to the change in threshold voltage, which ultimately becomes DIBL.

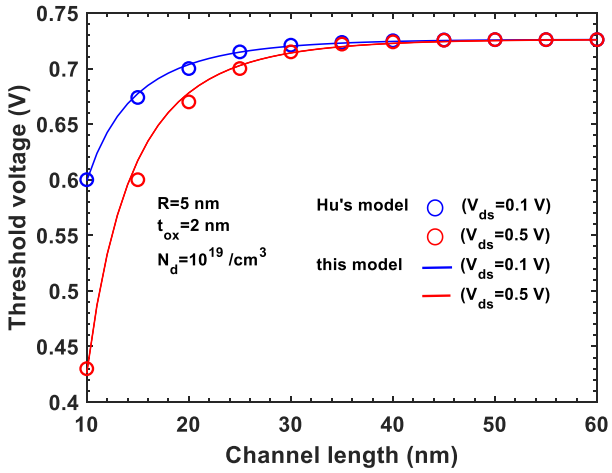

Figure 4. Comparisons of threshold voltages of this model and hu's model with drain voltage as a parameter under the given conditions in the figure.

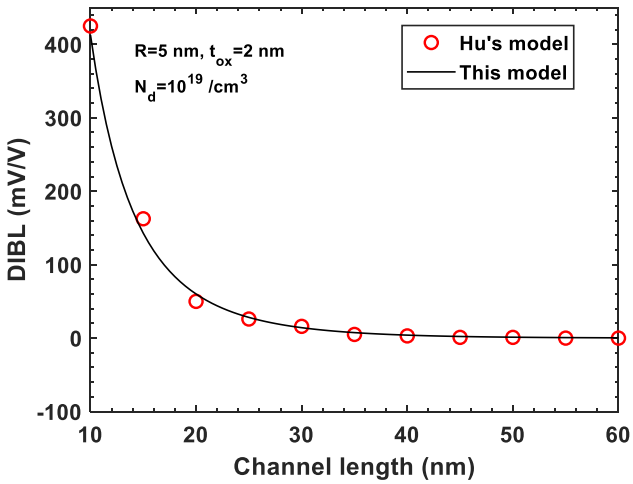

Figure 5. Comparisons of DIBLs of this model and Hu's model under the given conditions in the figure.

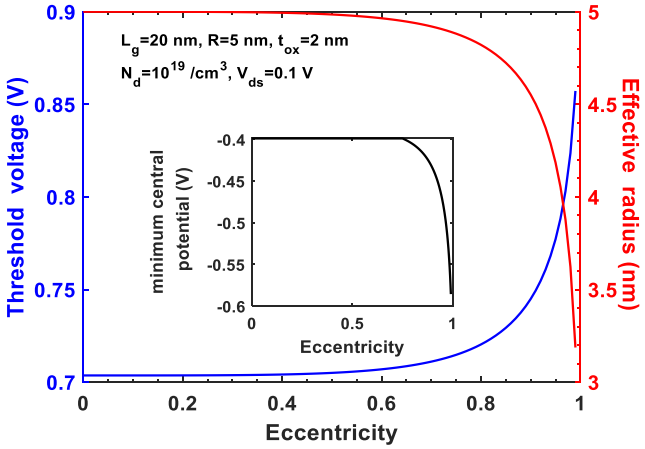

Figure 6. Threshold voltages and effective radius for the eccentricity under the given conditions in the figure.

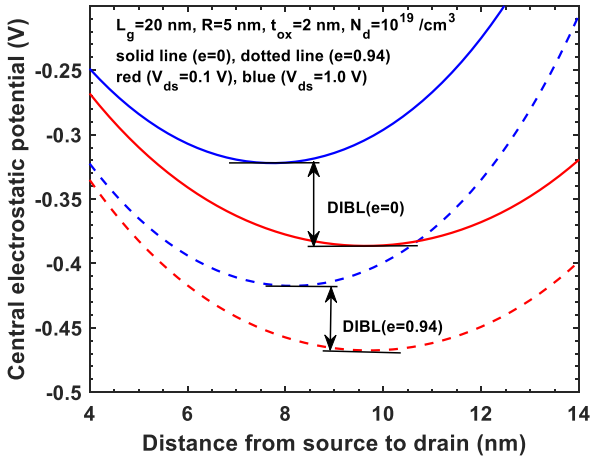

Figure 7. Central electrostatic potential distributions along channel length with the eccentricity and drain voltage as parameters under the given conditions in the figure.

To observe the change in DIBL for the eccentricity, the relationship between DIBL and eccentricity is shown in Fig. 8 using Eq. (9). In the inset of Fig. 8, the change in minimum central potential is shown for the eccentricity when the drain voltage is 0.1 V and 1.0 V based on Fig. 7. As shown in the inset of Fig. 8, the minimum central potential rapidly decreases for $e >$ 0.75 as the eccentricity increases under given conditions. In addition, when V_{ds} = 0.1 V and V_{ds} = 1.0 V, the difference in minimum central potential was compared at e = 0.2 and 0.9 by the size of the arrow in the inset of Fig. 8, and it was observed that the difference decreases as the eccentricity increases. Based on this, it can be seen that the DIBL shown in Fig. 8 also rapidly decreases above e = 0.75. As shown in Fig. 6, an increase in the eccentricity will appear as a decrease in the effective radius. DIBL is proportional to the square of the channel radius as can be seen in the previous paper [30], so DIBL also decreases sharply along with a decrease in the effective radius when the eccentricity increases. Comparing Fig. 6 and Fig. 8, it can be seen that a trade-off relationship is established between threshold voltage and DIBL. The specific values for the eccentricity from the threshold voltage and DIBL values shown in Figs. 6 and 8 are shown in Table 2 under the given conditions in the figures.

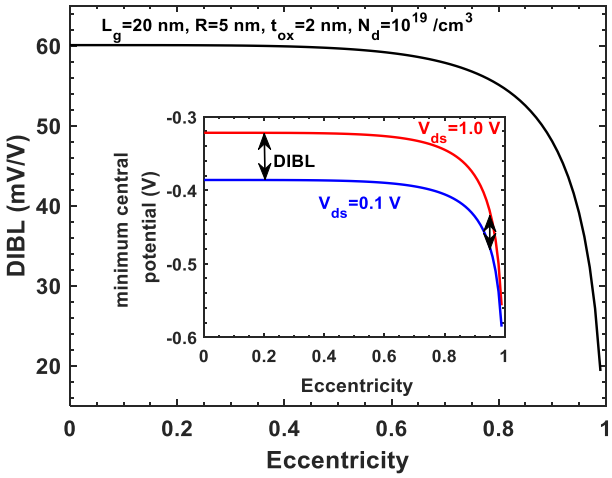

Figure 8. DIBL for the eccentricity under the given conditions in the figure.

Table 2. Threshold voltages and DIBLs for the specific eccentricity under the given conditions in Figs. 6 and 8.

Eccentricity	Threshold voltage [V]	DIBL [mV/V]
0.1	0.704	60.1
0.2	0.704	60.1
0.3	0.704	60.0
0.4	0.704	59.9
0.5	0.705	59.7
0.6	0.707	59.1
0.7	0.711	57.8
0.8	0.720	55.1
0.9	0.745	48.0
0.99	0.857	19.3

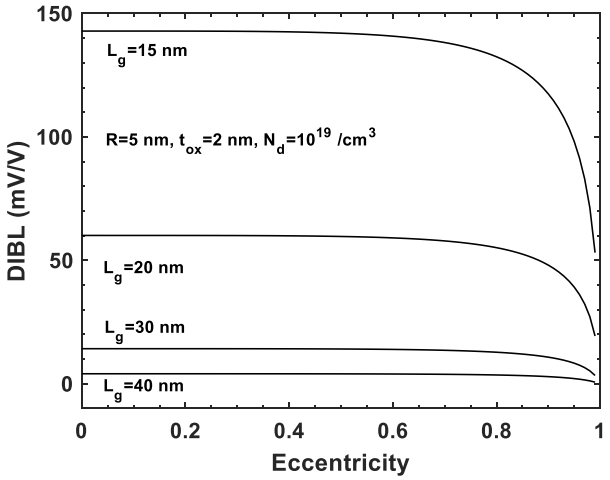

Figure 9. DIBLs for the eccentricity with channel length as a parameter under the given conditions in the figure.

To observe the change of DIBL according to the eccentricity with the channel length as a parameter, the results obtained using the presented DIBL model of Eq. (9) are shown in Fig. 9. It can be observed that the change of DIBL for the eccentricity decreases significantly as the channel length increases. In general, for the conventional MOSFET, DIBL is known to be proportional to L_a^{-n}, and $n = 3$ is usually [31]. In Fig. 9, for the circular GAA MOSFET with $e = 0$, it is roughly proportional to $n \approx 3$, but as the eccentricity increases, that is, the cross-sectional area changes to an ellipse, the change of DIBL with respect to the channel length decreases to $n < 3$. This shows that the change in cross-sectional area from a circle to an ellipse does not significantly affect the DIBL as the channel length increases.

Figure 10 shows the changes in DIBL according to the eccentricity for the channel radius and oxide thickness. In the case of the conventional MOSFET, DIBL is proportional to R^n for the channel radius R and generally $n = 2$ [31]. However, in the case of the circular GAA MOSFET, the n is between 1 and 2 [32], and it can be seen that this relationship is satisfied in Fig. 10(a) when $e = 0$. As the channel radius increases, the change in DIBL for the eccentricity is very severe, and it can be observed that it approaches $n \approx 1$. In addition, DIBL is linearly proportional to the thickness of the gate oxide, and this relationship is maintained regardless of the change in the eccentricity as shown in Fig. 10(b). That is, it can be seen from Fig. 10(b) that the change in DIBL for the eccentricity is almost constant when the gate oxide thickness changes.

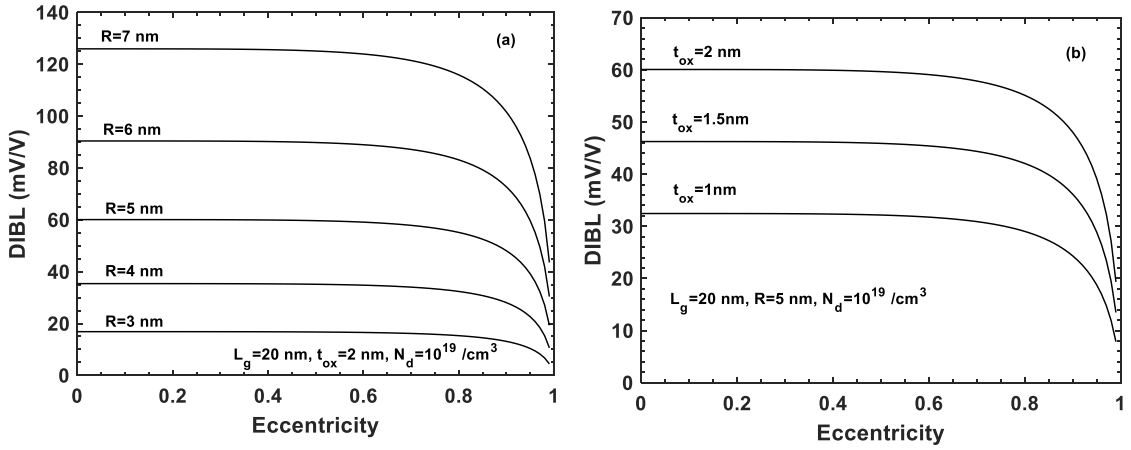

Figure 10. DIBLs for the eccentricity with (a) channel radius and (b) oxide thickness as parameters under the given conditions in the figure.

4. CONCLUSIONS

In the case of the elliptic junctionless GAA FET, the threshold voltage and DIBL were analyzed and compared with those of the circular GAA FET. For this purpose, the analytical threshold voltage and DIBL models were presented, and it was observed that the result was in good agreement with the results of other papers already verified. The threshold voltage and DIBL were compared for cases with the same cross-section area when the cross-section changed from circular to elliptic, and the changes in threshold voltage and DIBL were observed for changes in the eccentricity of the ellipse. Since it is difficult to manufacture a GAA FET with an accurate circular structure, research on GAA FETs with an elliptic cross-section is considered

very important. As a result of calculations using the analytical threshold voltage and DIBL models presented in this paper, it was observed that as the eccentricity increases, the threshold voltage increases while DIBL decreases. However, there was no significant change in the threshold voltage and DIBL until the AR was about 1.5 corresponding to the eccentricity of about 0.75, and it was observed that there was a significant change in the threshold voltage and DIBL when the eccentricity increased above 0.75. This is believed to be due to a change in minimum central potential distribution and a decrease in R_{eff} as the eccentricity increases. The absolute value of the minimum central potential in the channel increased and the threshold voltage increased as the eccentricity increased. In addition, the absolute value of the minimum central potential decreases as the drain voltage increases, thereby decreasing the threshold voltage, and the decreasing rate reduces as the eccentricity increases, so it was found that DIBL ultimately decreases as the eccentricity increases. Therefore, threshold voltage and DIBL showed a trade-off relationship for the eccentricity. It was observed that the rate of change of DIBL for eccentricity decreases as the channel length of the elliptic GAA FET increases and the channel radius decreases and that the change in oxide thickness has little effect on the change in DIBL for eccentricity.

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CRediT authorship contribution statement. Hakkee Jung: Methodology, Investigation, Formal analysis.

Declaration of competing interest. The authors declare no conflict of interest.

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