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HETEROGENEOUS INTEGRATION APPROACH BASED ON FLIP-CHIP BONDING AND MISALIGNMENT SELF-CORRECTION ELEMENTS FOR ELECTRONICS-OPTICS INTEGRATION APPLICATIONS

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Abstract. This paper presents a high precision bonding approach, capable of submicron alignment accuracy, based on the thermosonic flip-chip bonding technique and misalignment self-correction elements. The precision of the bonding technique is guaranteed by using of misalignment self-correction bump (convex) and hollow (concave) elements. Metal cone bump and conductive sloped hollow bonding pad elements are created using micro-machining techniques, on a chip specimen and substrate, respectively. The chip and substrate are bonded face-to-face using of an ultrasonic-enhanced flip-chip bonder. By introducing of misalignment self-correction elements, repeatable bonding accuracies of less than 500 nm were confirmed through experimental investigation. Bond properties, including electrical and mechanical properties, are also characterized to confirm the success of the bonding approach. With the obtained results, the proposed bonding approach is capable of being use in electronics-optics heterogeneous integration applications.

Keyword: photonic-electronic convergence system technology (PECST), flip-chip bonding, misalignment self-correction elements.

1. INTRODUCTION

In recent years, much research has been focused on the development of photonics-electronics convergence system technology (PECST), the integration technology would helps to overcome the limitations of power minimization, operating speed acceleration and down-sizing of the current LSI technology [1–5]. Using this technology, electrical, mechanical, optical, and passive devices and components are highly integrated to form low power consumption, high-speed, high-performance systems.

In photonics-electronics heterogeneous integration applications, the optical performance of a system is highly dependent on the coupling technique. Matching the light field of a component to the mode field of another component (e.g. from an exciter to a waveguide, as shown in Fig. 1) is needed for efficient transferring of optical energy. The

coupling efficiency is mainly affected by the numerical aperture of waveguides, refractive index changes, longitudinal and transverse offsets ($\Delta x, \Delta y, \Delta z$), and angular offset ($\Delta\theta$), in which losses due to the offsets are critical [6]. Therefore, improvement of the integration accuracy has been being under investigation of several research groups [4, 7, 8].

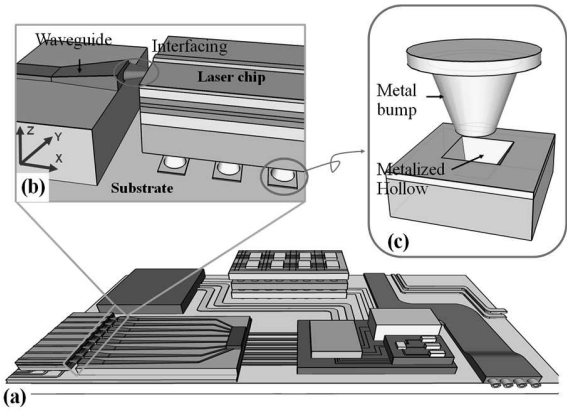

Fig. 1. Concept of electronics-optics heterogeneous integration.

To implement the heterogeneous integration, flip-chip bonding (FCB) has been a promising technique for high density interconnections with simple processes [9, 10]. However, commercialized FCB machines to date have been limited the bonding accuracy to the range of 2 μm – 5 μm, because of unwanted effects such as thermal-induced misalignment due to mismatched thermal expansion of the chip and substrate, or by having the bonding surface slide out by the shear force of the large downward force during bonding [11]. Improvement of the bonding accuracy through increasing the resolution of the alignment stage motion and increasing the magnification of the IR image camera is not sufficient.

Our work deals with effectively improving the conventional ultrasonic-enhanced FCB approach through modifying the bonding bump and pad elements used in FCB to form a misalignment self-correction structure pair, to achieve time-efficient bonding approach with sub-micron range precision bonding.

2. BONDING APPROACH BASED ON MISALIGNMENT SELF-CORRECTION ELEMENTS

FCB has been widely used in many applictions to stack chips in different materials and fields together [10]. In FCB, the most commonly used method is supplying thermal energy to material bumps and pads which are under compression for the forced contact of the bonding surfaces (thermocompression bonding - TCB method) [12]. However, the TCB process often has problems such as large thermal deformations of the assembly or long process time. Ultrasonic-enhanced flip-chip bonding (US-FCB) is developed from TCB and ultrasonic weding [13]. US-FCB replaces a part of the thermal bonding energy and the mechanical deformation energy in TCB with ultrasonic energy in making a bond. This substitution allows metal-to-metal interconnections to be made in shorter time (normally

from 500 ms to few seconds), and at lower temperatures (below 150°C). Due to its advantages in decreasing processing temperature and processing time, the US-FCB process has been used in integration and packaging technologies [14, 15].

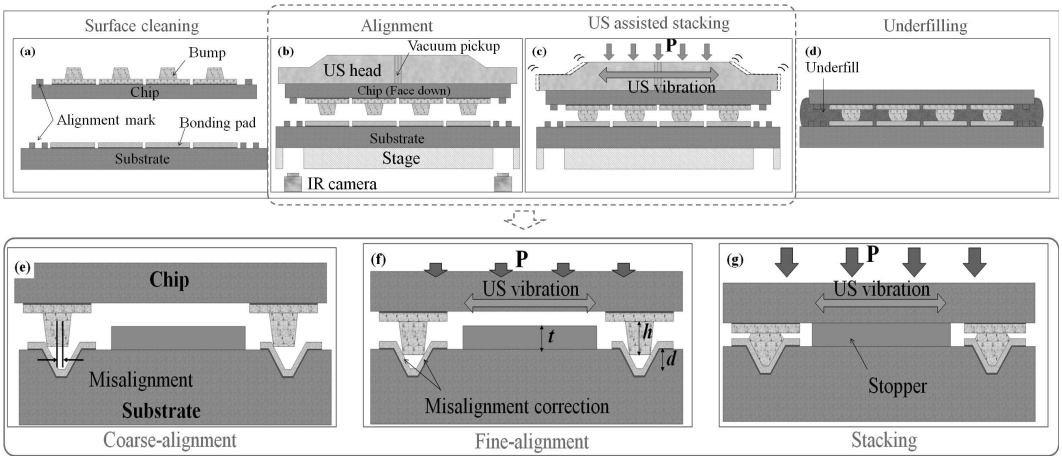

Fig. 2. Schematic view of proposed modified USB using misalignment self-correction elements (MSCEs).

The conventional US-FCB procedure is shown in Fig. 2 (a-d) and can be described as follows. The surfaces of Au bumps and pads are first cleaned using Argon plasma (Fig. 2 (a)). The stacking procedure begins with the substrate being placed on a stage and fixed to the stage by a vacuum. The chip is picked up from the chip tray and is brought into alignment with the substrate (Fig. 2 (b)). A bonding load and ultrasonic power is simultaneously applied to the chip. Bumps on a chip and pads on a substrate are contacted under bonding force. Ultrasonic vibration energy is then applied to the bonding interface to remove the surface oxides or the contamination of the bumps and the pads and to form microwelding with strong bonding strength at bonding interface (Fig. 2 (c)). The bonded area is finally filled with an underfilling material, a resin strengthening agent, and heated to be hardened (Fig. 2 (d)).

To improve the accuracy of the bonding process, we propose misalignment self-correction elements (MSCEs) which are utilized to correct and maintain the alignment of chip to substrate during staking, automatically [16]. The MSCEs are based on the principle of using bump (convex) and hollow (concave) elements (Fig. 1 (c)) for alignment purpose.

In this modified bonding approach, metal bumps and pads with metalized cavity (hollow concaves) are also placed on the chip and substrate. The chip is flipped and bonded face-to-face with the substrate. Offsets $\Delta x, \Delta y$ in x- and y-axis, and angular offset $\Delta\theta$ are determined by the bump and hollow pair structure while the offset in the z direction Δz is decided by controlling the bonding conditions, along with mechanical stoppers. Bump and cavity structures provide mechanical guides for maintaining high precision alignment between the interconnect pads during the bonding process. The chip is aligned with the substrate as usual (Fig. 2 (e)), i.e. coarse alignment. After that, the sloped sidewalls of

the dielectric pyramids help guide the top die cone bumps to the substrate bonding target (Fig. 2 (f)), i.e. fine alignment. Under the vertical down-force when the two dice brought together, bump-cavity structures slide into each other in a horizontal direction to correct the misalignment, if there is one. Bonding conditions (i.e. US power, temperature, pressure, time) are applied to create a strong stacking (Fig. 2 (g)).

3. FABRICATION OF TEST SAMPLES

For demonstrating the bonding approach, chip specimens with dimensions of 0.5 mm × 2 mm × 0.38 mm and substrates of 10 mm × 10 mm × 0.380 mm (width × length × thickness) were fabricated in Si (Fig. 3). Au hollow pads, with a slope angle of 54.7°, were micro-machined on substrates using a wet anisotropic (TMAH) etching process and a vacuum deposition process, while gold bumps were deposited on an under bump metal layer (UBM) on chip specimens. Cu deposited stoppers were placed on the substrate for limiting the gap between chip and substrate. The fabricated chip specimen and substrate are shown in Fig. 4(a, d). The fabricated hollow cavities on a chip and cone bumps on a substrate are depicted in Fig. 4(b, e). Fig. 4(c, f) are the sketches of cross-sectional view of bump and hollow pad.

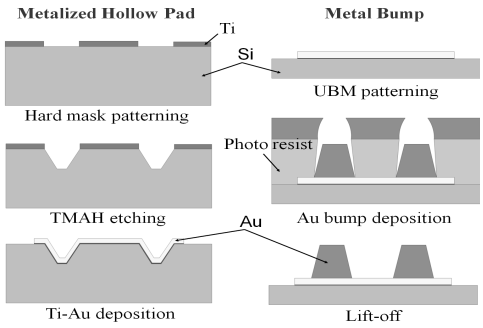

Fig. 3. Fabrication process of hollow pads and metal bumps.

Table 1. Test specimen parameters.

Parameters of bumps on the chip specimens		Parameters of hollow bonding pads on the substrates	
Bump height (h)	Bump diameter ($\varnothing$)	Cut-out width (w)	Hollow depth (d)
5.5 μm	10 μm	12 μm	3 μm

Parameters of bumps and hollow pads which are used in the experiments are listed in Tab. 1. The size of the cavity are made to be larger than bumps diameter to guarantee that bumps can be inserted into the cavity pads, regardless of a few micrometers of misalignment between them that may occur after coarse aligning. The total number of cone

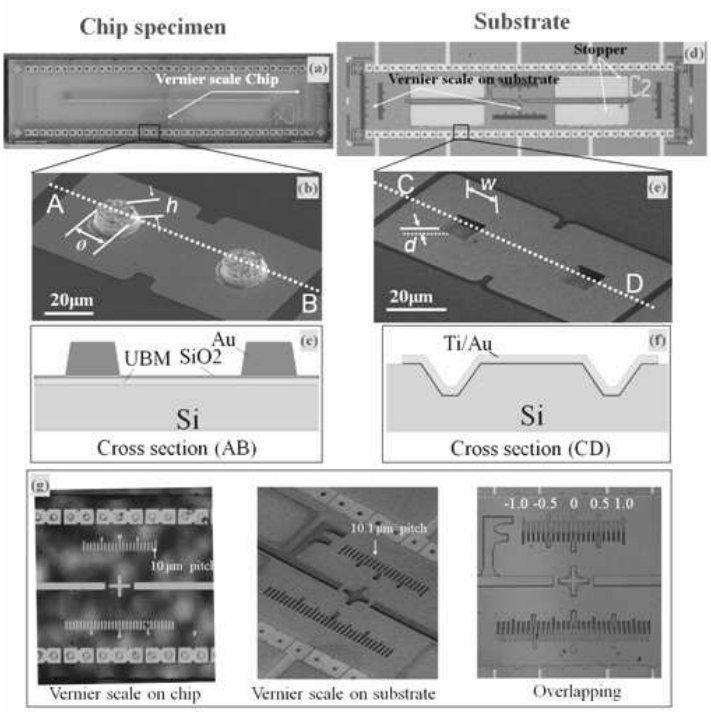

Fig. 4. Fabricated test samples.

bump-hollow concave pairs in this design is 80. Bumps and pads are connected to form a daisy-chain for electrical test of the bonding interconnections. In order to evaluate the bonding accuracy, vernier scales in x- and y-axis (see Fig. 4(g)), with the finest resolution of 100 nm, were also designed and formed during the fabrication process.

4. EXPERIMENTAL RESULTS AND DISCUSSION

The bonding process was implemented with a flip-chip bonder of Bondtech Co., Ltd., CA-300. The original TCB head was replaced with an ultrasonic horn for USB. First, bonding conditions were evaluated by stacking chip specimens to substrates which having conventional flat bonding pads. Both electrical and mechanical properties of the stacking were taken into consideration.

Bonded chips were subjected to shear testing for evaluation of the bond strength. The bonded samples were placed on a stage in such a way that the substrate was held by a metal stopper to limit its lateral movement, while the top chip was pushed parallel to the sample surface. To avoid friction between the shearing blade and the substrate surface, a small gap was inserted between them. The blade slowly traveled until fracture was detected as a sudden drop in applied force. The force acquired during the test was recorded to determine the maximum applied force, i.e. the bond strength. Tab. 2 lists the bonding conditions after optimized for desired stacking and bump height. The average

bonding shear strength was estimated to be 4.5 N. The bump height after bonding was smaller than the total of the cavity pad depth and the stopper height.

Table 2. Bonding conditions after optimization.

Parameter	Value	Units
Pressure	15	MPa
US vibration amplitude	2.2	μm
US frequency	48.5	kHz
Bonding time	500	μs
Temperature	300	K

Fig. 5 shows the electrical performance of the interconnections characterized by taking the I-V characteristics of the daisy-chain. Average resistance of the cone bump and hollow concave connection was calculated to be 0.3 Ω. The linearity of the I-V curves confirmed the perfect Ohmic contact of the connections.

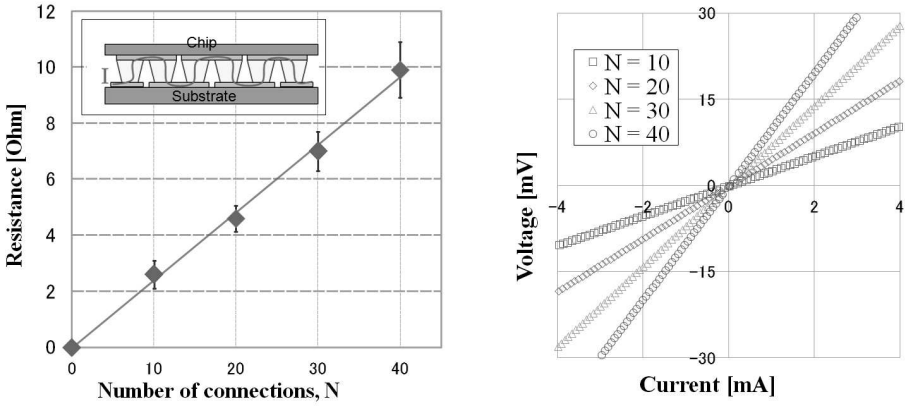

Fig. 5. Electrical properties of the bonding interconnection. (a) The inset shows the Daisy-chain diagram. (b) I-V char-acteristics of the interconnections.

The bonding accuracy was also examined on these samples through the designed vernier structures which were created at the bonding interface. The observed bonding accuracy results are shown in Fig. 6. Due to the bonding head vibrates in the y direction, the post-bond offsets in this direction are larger than in x direction, and are within the range of ± 5 μm.

The optimized bonding conditions after that were applied to the chip and substrate with proposed MSCEs and bonding accuracy was evaluated. Fig. 7(a, b) shows the infrared images through a chip after alignment and stacking. We could see that the chip was aligned with the substrate under the assistance of bump and cavity pair structures, resulting in high-precision bonding, i.e. less than 500 nm in transverse offsets. Besides, the bonding

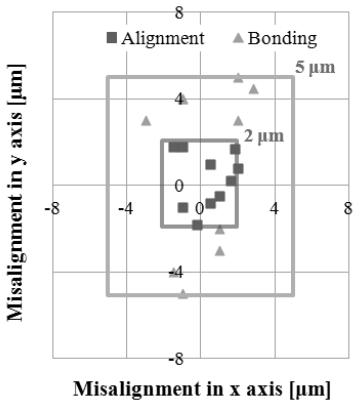

Fig. 6. XY alignment and bonding offset of the bonding machine before using MSCEs.

time was the same as a usual USB process (i.e. without using of alignment self-correction structures).

The bonded chips were subjected to cross-section inspection to examine the deformation of the gold bump. The cross-section image of a bonded bump in Fig. 7(c) verifies that the offset result in Fig. 7(b) is due to the misalignment auto-correction effect of the bumps and cavity structures.

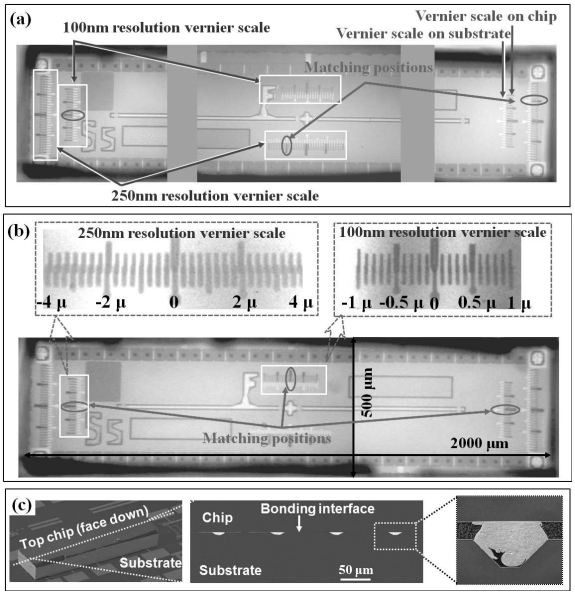

Fig. 7. Bonding accuracy result. IR images illustrate the tolerance after alignment (a) and bonding (b) pro-cesses. (c) is the cross section view showing the bonding interface.

For an actual application, remarks about the size of the MSCES and parallelism of the bonding chip–substrate are considered. The size of the bumps should be large enough so that are not broken during self-alignment period. It can be seen that, a given certain hollow bonding pad, the bigger the bump size, the stronger the shear strength of the bump. However, the bumps' size should be traded off so that they can be inserted to the hollow pads regardless of a few micrometers misalignment between them that may occur. In our experimental results we confirmed that MSCEs work well with a bump size 2 μm smaller than the size of the hollow pad.

Additionally, if the parallelism of the chip and substrate surfaces is imperfect, the initial contact will take place at an edge, and stress will cause slippage in the lateral direction and may course a large offset. Therefore, it is necessary to carefully calibrate the parallelism of the picked-up chip and substrate surface before bonding.

5. CONCLUSIONS

A modified USB process has been presented. By using of low-temperature bonding approach based on US-FCB and modifying of the bonding bump and pad elements to form MSCEs, the conventional flip-chip bonding process was improved in term of alignment accuracy and time-efficiency. The test chips with micro Au bumps and substrates with hallow bonding pads were fabricated and bonded face-to-face. We could confirmed the bonding accuracy of a conventional bonding approach in the range of a few micrometers was improved to sub-micrometer range by applying the new approach. With the initial obtained results, the bonding approach is capable of achieving high-precision bonding at low-temperature and therefore it can be employed in electronics-optics heterogeneous integration.

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