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ROLES OF GATE-OXIDE THICKNESS REDUCTION IN SCALING BULK AND THIN-BODY TUNNEL FIELD-EFFECT TRANSISTORS

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ABSTRACT

Tunnel field-effect transistor (TFET) has recently been considered as a promising candidate for low-power integrated circuits. In this paper, we present an adequate examination on the roles of gate-oxide thickness reduction in scaling bulk and thin-body TFETs. It is shown that the short-channel performance of TFETs has to be characterized by both the off-current and the subthreshold swing because their physical origins are completely different. The reduction of gate-oxide thickness plays an important role in maintaining low subthreshold swing whereas it shows a less role in suppressing off-state leakage in short-channel TFETs with bulk and thin-body structures. When scaling the gate-oxide thickness, the short-channel effect is suppressed more effectively in thin-body TFETs than in bulk devices. Clearly understanding the roles of scaling gate-oxide thickness is necessary in designing advanced scaled TFET devices.

Keywords: gate-oxide scaling, SOI structure, short-channel effect, low-bandgap device, tunnel field-effect transistor (TFET).

1. INTRODUCTION

In order to reduce the power consumption of electronic devices, one needs scaling down supply voltage because the dynamic power consumption of integrated circuits is a quadratic function of applied voltage [1]. For that purpose, tunnel field-effect transistor (TFET) has been recognized as a feasible choice since its subthreshold swing at room temperature is able to be less than 60 mV/decade which is a physical limit of conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) [2 - 4]. The steep subthreshold swing of TFETs is a fundamental advantage to allow of scaling down the supply voltage while still keeping an acceptable drive current [5, 6]. The essential difference between TFETs and MOSFETs is that the conduction current in TFETs is generated by the band-to-band tunneling (BTBT) of valence electrons from the source to the drain [7], whereas the mechanism of electrical transport in

MOSFETs is the injection of free electrons through a thermal energy barrier [2]. Because of this new conduction mechanism, TFET devices are not under the Boltzmann limit of 60 mV/decade subthreshold swing [8]. Since the BTBT probability is exponentially inverse-proportional to the energy bandgap, using low-bandgap semiconductors is the most effective method to achieve a sufficiently high on-current for the practical applications of TFETs [9, 10].

Similar to MOSFETs, the role of gate terminal in TFETs is also to control the potential profile in the channel region to establish the on- and off-states of transistors [7]. Because the channel potential is induced by the gate field through the gate-oxide layer, the gate-oxide thickness is an important factor in determining the on-off switching of TFETs. Previous works have shown that the on-current and subthreshold swing of TFETs depend significantly on electrical oxide thickness (EOT) [11-13]. Particularly, decreasing the EOT makes the on-current increased [12] and the subthreshold swing decreased [11, 13], regardless of point- or line-tunneling TFET architecture. The improvement of TFET performance with scaling the EOT is positively attributed to the higher gate control capability which results in the stronger and faster on-off transition of tunnel barrier. Both analytical and numerical results have also shown that the reduction in EOT is useful in containing short-channel effects in double-gate TFETs to allow of scaling the feature size down to 30 nm [14 - 16]. However, the roles of gate-oxide thickness reduction in scaling bulk TFETs have not been investigated properly. Furthermore, an adequate comparison on the roles of gate-oxide scaling in suppressing short-channel effects in bulk and thin-body TFETs is necessary for understanding their device physics and guiding the design rules of this advanced transistor.

In this study, we properly examine and compare the roles of gate-oxide thickness reduction in scaling low-bandgap germanium TFETs with bulk and thin-body architectures. The bulk structure is a single-gate TFET and the thin-body structure is a silicon-on-insulator (SOI) single-gate TFET. The electrical characteristics of TFETs are produced by using two-dimensional device simulations [17]. The paper consists of four sections, including the Introduction (section 1) and the Conclusions (section 4). Section 2 describes the device structures and physical models used in the simulations. The detailed investigations of short-channel effects depending on EOT in bulk and thin-body TFETs are presented in main section 3.

2. DEVICE STRUCTURES AND SIMULATION MODELS

Figure 1 shows the schematic views of homojunction Ge single-gate TFETs with bulk and thin-body structures. For the practical significance of the study, low-bandgap germanium (Ge) was adopted since using low-bandgap semiconductors has been known as the most effective technique to boost the on-current of TFETs. In order to exactly elucidate the roles of gate-oxide thickness reduction in scaling TFETs, a basic homojunction structure was chosen to eliminate the influences of material and structure parameters. The bulk and thin-body structures are investigated simultaneously because their different gate-controlled bodies may lead to the significantly different effects of the gate-oxide thickness on the device scalability. The drain of TFETs was lightly doped with a donor concentration of 10^{18} cm^{-3} for minimizing the ambipolar off-leakage [18], whereas an n-type doping concentration of 10^{17} cm^{-3} was defined in the channel region. The electrical oxide thickness of high-*k* gate-dielectric HfO_2 was suitably varied for studying purposes. The doping gradient with a Gaussian profile was set at a practical value of 2 nm/decade. The gate workfunction of 4.2 eV was fixed in all simulations. For thin-body TFETs, a 10 nm body thickness was used to maximize the tunneling current density [19] and to minimize the quantum mechanical effects [20, 21].

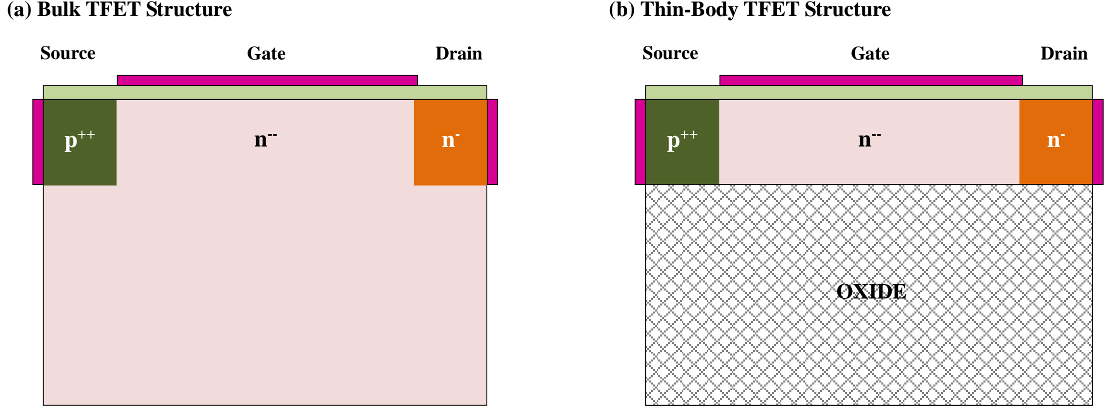

Figure 1. Schematic structures of low-bandgap germanium tunnel field-effect transistors with (a) bulk and (b) thin-body structures.

The electrical characteristics of TFETs and associated physical explanations were provided by two-dimensional device simulations [17] with appropriate models and parameters. Since the direct BTBT dominates the conduction current in TFETs based on relaxed Ge [22], the nonlocal direct-tunneling Kane model is applied to determine the tunneling generation rate in TFETs as [23]:

$$G_{\mathrm{BTBT}} = A\frac{\xi^2}{E_g^{1/2}}\exp\left(-B\frac{E_g^{3/2}}{\xi}\right), \quad (1)$$

where E_g is the material bandgap and ξ is the nonlocal electric field at tunneling junction. Parameters A and B which depend on electron and hole effective masses of semiconductors can be input easily in the simulations. We have calculated A and B to get 1.6×10^{20} eV$^{1/2}$/cm.s.V^2 and 9.5×10^6 V/cm.eV$^{3/2}$ respectively. Compared to the experimentally calibrated value of 9.0×10^6 V/cm.eV$^{3/2}$ [24], our calculation of parameter B is only about 5 % of deviation after including the effect of heavy-doping bandgap narrowing [17]. This small deviation is mainly due to the uncertainty of the used effective masses. It is difficult to confirm whether parameter A is experimentally appropriate or not because there is no method good enough to extract the value of A from experimental data. Fortunately, the BTBT generation is much more sensitive to B than to A, only experimentally calibrated B can also certify the acceptable validity of the tunneling model [24]. In addition, the Fermi-Dirac distribution and Shockley-Read-Hall (SRH) recombination were also incorporated for more realistic simulations.

3. EFFECTS OF ELECTRICAL OXIDE THICKNESS ON DEVICE SCALING

Since the gate control capability is directly related to gate-oxide layer, scaling the EOT is an efficient approach to improve the on-off switching of not only conventional MOSFET but also TFET devices. Because the slope of current-voltage curves is almost a constant in the subthreshold region, the short-channel effect of classical MOSFETs can be evaluated by simply considering the subthreshold swing. For TFETs, however, the subthreshold swing is a strong function of gate voltage [8]. In this section, therefore, the effects of EOT on the short-channel effects of bulk and thin-body TFETs are explored by analyzing both the subthreshold swing and off-current to elucidate the roles of the EOT reduction to their scalabilities.

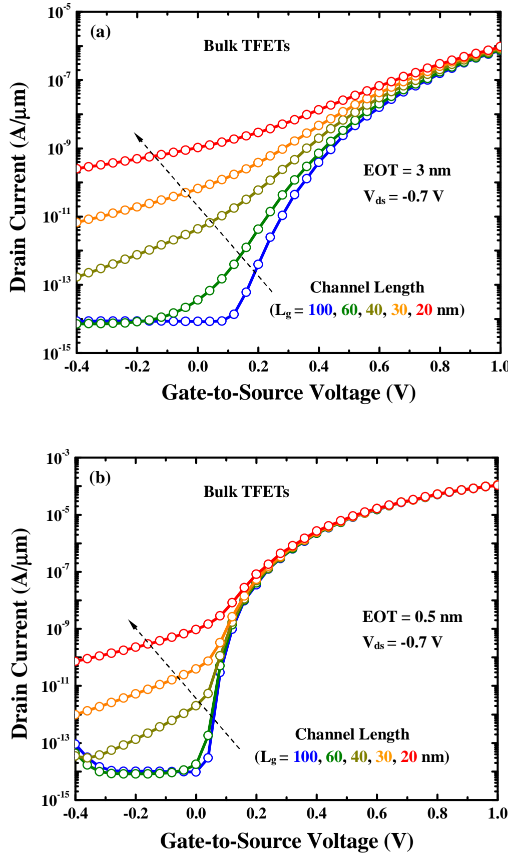

Figure 2. Gate transfer characteristics for bulk TFETs with (a) EOT = 3 nm and (b) EOT = 0.5 nm as a function of channel length (L_g).

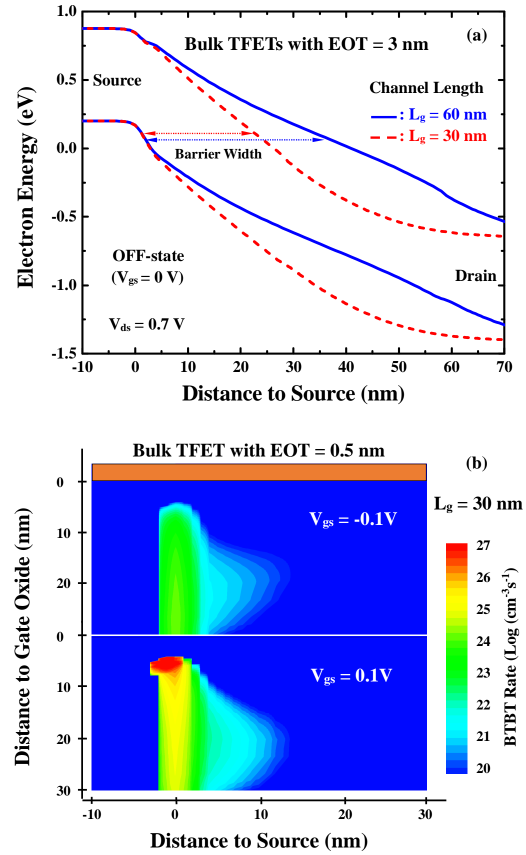

Figure 3. (a) Off-state energy-band diagrams of bulk TFETs with different channel lengths, (b) BTBT rates of 30nm bulk TFET at different gate.

3.1. Bulk TFET structure

Figure 2 presents the current-voltage characteristics of bulk TFETs with various channel lengths ranging from 100 to 20 nm and two values of EOTs. The on-current of TFETs is significantly enhanced by decreasing the EOT from 3 to 0.5 nm, particularly two orders of magnitude. This on-current enhancement is surely attributed to the increase in the gate control capability which determines the tunnel barrier width at the source-channel tunneling junction. In subthreshold regions, in general, the short-channel effects are clearly observed in both the thick and thin EOT TFETs when scaling the channel length down to 20 nm. However, the short-channel effect in the EOT = 3 nm TFETs is slightly more pronounced than that in the EOT = 0.5 nm TFETs. With EOT = 0.5 nm, the channel length of the bulk TFETs can be scaled down to 60 nm without short-channel effects, whereas that limit of the channel length is 100 nm with EOT = 3 nm. Notably, while the tunneling current in the EOT = 3 nm TFETs increases regularly with increasing gate voltage, there is a clear knee in the subthreshold region of the current-voltage curves of the short-channel TFETs with EOT = 0.5 nm. The knee point separates the high swing and low swing regions in the subthreshold regime of TFETs.

Although the fact that the short-channel performance is better in the thinner EOT TFETs is

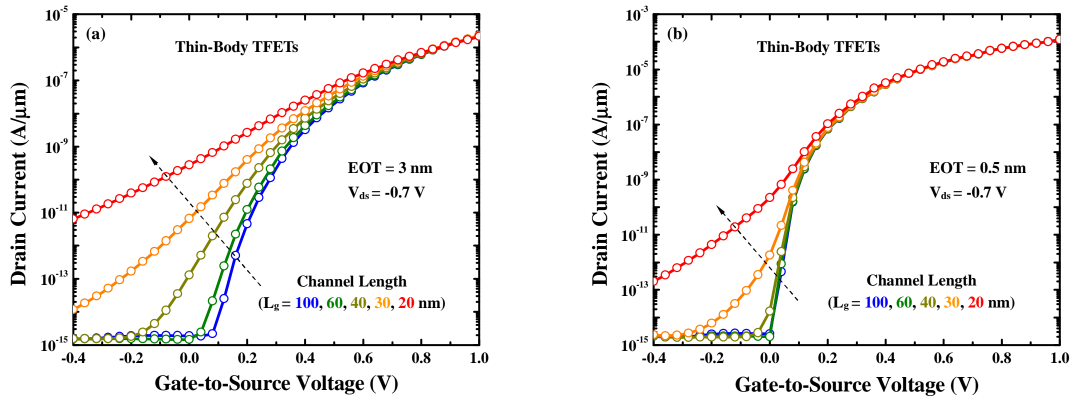

Figure 4. Current-voltage curves of thin-body TFETs with (a) EOT= 3 nm and (b) EOT = 0.5 nm for various channel lengths (L_g).

obviously ascribed to the strengthened capability of gate control, it is important to realize that the improvement in short-channel effect when decreasing EOT is the result of combining two different effects. The first one is that with the thinner EOT, the gate can effectively control the deeper range of the channel. Since the high subthreshold current caused by short-channel effect is mostly generated at the region far from gate, the subthreshold current is decreased with decreasing the EOT. The second effect is related to the on-state tunneling onset voltage which is defined as the gate voltage when the tunneling at the upper right edge of source begins. The onset voltage decreases with decreasing the EOT because an increased capability of gate control results in a larger band bending at source-channel junction. The premature on-state tunneling onset indirectly assists in decreasing the subthreshold current and swing because the on-state tunneling onset occurs at the gate voltage that the leakage tunneling current is still small.

In order to explain the short-channel effect of bulk TFETs, Figure 3(a) plots the off-state energy-band diagrams of bulk TFETs with different channel lengths. The energy-band diagrams are intentionally extracted along a lateral cut-line that is 20 nm far from the gate-oxide because the off-leakage current is almost contributed by the tunneling at that region. For the short channel of 30 nm, the tunnel barrier width is considerably small compared to that of the 60nm TFET. This smaller tunnel width results in a higher tunneling probability and thus a larger tunneling leakage current and subthreshold swing. Because the basic physical mechanism of short-channel effect does not depend on gate-oxide thickness, the above explanation is also applied for the TFETs with EOT = 0.5 nm. To physically understand the existence of the knee point and the property of the onset voltage in the bulk TFETs with thin EOTs, Figure 3(b) shows the BTBT generation rates of the bulk TFET with the EOT of 0.5 nm at different subthreshold voltages. At the gate voltage of -0.1 V, the BTBT generation at the lower region, which is far from the gate, is large and thus dominates the subthreshold tunneling current. Because this region is weakly controlled by the gate, the subthreshold swing at this voltage is very large. When the gate voltage reaches to 0.1 V, the BTBT generation at the upper left edge of channel is much larger than that at the remaining region. Because the upper left edge of channel is right beneath the gate-oxide, it is the most strongly gate-controlled region. Therefore, the subthreshold swing at this voltage is low. Because it has to exist an onset voltage of the tunneling at the upper left edge of channel, there definitely is a knee point at which the subthreshold swing varies abruptly. However, if the EOT is large, the gate control on this region is relatively weak and therefore the subthreshold swing at the gate voltage of 0.1 V is comparable to that at the gate

voltage of -0.1 V. Consequently, no knee point is observed in the current-voltage curves of bulk TFETs with 3nm EOT as mentioned previously in Figure 2(a).

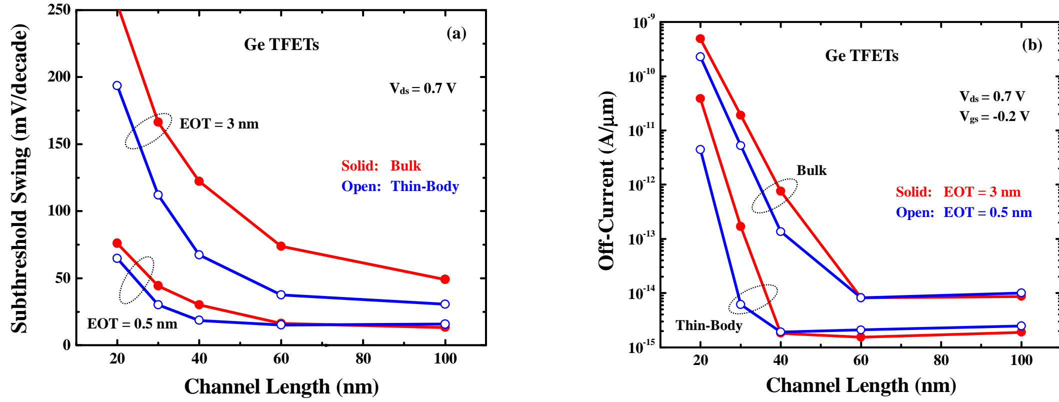

Figure 5. (a) Minimum subthreshold swing and (b) off-current as a function of channel length of bulk and thin-body TFETs with different electrical oxide thicknesses (EOT).

3.2. Thin-Body TFET structure

The analyses in the previous section show that the subthreshold current of TFETs is largely contributed by the tunneling at the channel region far from the gate-oxide. Therefore, it is expected that the scaling of body thickness is probably helpful significantly in suppressing the short-channel effect of TFETs. To examine the dependence of short-channel effects on the EOT in thin-body TFETs, Figure 4 shows the current-voltage characteristics of 10nm body TFETs with different EOTs. The short-channel effects are still observed when scaling the channel length down to 20 nm. For the EOT of 3 nm, the short-channel effect is severe in sub-60 nm TFETs. Compared to the bulk TFET structure, using the thin-body structure for TFET devices makes the device scalability increased. Particularly, the thin-body TFETs can be scaled to 60 nm without appreciable short-channel effects, whereas that length of the bulk counterparts is 100 nm. For the EOT of 0.5 nm, the off-current and subthreshold swing of TFETs are only degraded when the channel length is scaled below 40 nm. This scaling limit of the thin-body TFETs is also smaller than that of the bulk devices which is shown in the previous section to be 60 nm. The better short-channel performance in the thin EOT TFETs compared to the thick EOT devices is still related to the roles of the gate control on the channel region. The significantly improved scalability of TFETs by using the thin-body structure is due to the reduction of the off-state tunneling region that is far from the gate-oxide. As seen in Figure 3(a), if the body thickness is decreased, the area of off-state tunneling generation which causes short-channel effects is decreased accordingly. Therefore, scaling EOT is more efficient in suppressing short-channel effect in thin-body TFETs than in bulk devices.

Up to now, one still thinks that the minimum subthreshold swing is a good indicator to reflect the on-off switching and associated short-channel effect of TFETs. To inspect this point of view and to explicitly understand the roles of EOT reduction in scaling TFET devices, figure 5 depicts the minimum subthreshold swing and off-current as a function of the channel length for bulk and thin-body TFETs with thick and thin oxide layers. Generally, the subthreshold swing and off-current are considerably degraded with decreasing the channel length of the bulk and thin-body TFETs below 60 nm. In Fig. 5(a), the subthreshold swing is stronger dependent on the EOT than on the structure parameter. Namely, for both the bulk and thin-body TFETs, the

decrease in the EOT from 3 down to 0.5 nm results in the strong decrease in the subthreshold swing. For a given EOT value, however, the subthreshold swing is only slightly decreased by changing from the bulk to the thin-body structure. Although using the thinner body can also help to ameliorate the subthreshold swing, scaling body thickness is not as effective as decreasing gate-oxide thickness. As seen in Figure 5(b), on the other hand, the use of thin-body structure is more effective than scaling gate-oxide layer in term of diminishing off-current. For example, scaling the EOT from 3 to 0.5 nm makes the off-current of the 30 nm bulk TFET decreased about two times, whereas using the thin body of 10 nm can reduce the off-current of the EOT = 3 nm TFET approximately two orders of magnitude. Therefore, only looking at the minimum subthreshold swing is not enough to exactly estimate the short-channel effect of TFETs. This is because the minimum subthreshold swing is usually dominated by the tunneling at the upper left edge of channel where the gate control depends most strongly on the oxide thickness. On the contrary, the off-current is primarily contributed by the tunneling at the region far from gate, where the gate control capability is weakest. These different physical origins of the minimum subthreshold swing and off-current result in the knee points of current-voltage curves. Phenomenologically, whenever knee points are observed in current-voltage curves, considering the minimum subthreshold swing only cannot provide an accurate evaluation on the short-channel performance of TFETs.

4. CONCLUSION

The roles of gate-oxide thickness reduction in scaling TFETs have been adequately examined by analyzing the numerical simulations of the two-dimensional device structures. The physical mechanisms of the off-current and subthreshold swing have been clarified to highlight the different effects of scaling the EOT and body thickness on the short-channel effect of TFETs. The off-current and subthreshold swing have to be simultaneously considered when designing the gate-oxide layer and the body thickness to optimize the short-channel performance of TFET devices.

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