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BROADBAND GaAs pHEMT LNA DESIGN FOR T/R MODULE APPLICATION

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ABSTRACT

In this paper, a three stages monolithic low noise amplifier for T/R module application is presented. This amplifier is fully integrated on 0.15 µm GaAs pHEMT technology and achieves a wide bandwidth from 6 to 11 GHz. Within this band, the LNA has the minimum of 1.3 dB noise figure and over 25 dB small signal gain. The output third-order intercept point is over 30 dBm and the 1 dB compression point (P_{1dB}) is 16 dBm at the output.

Keywords: LNA; T/R Module; X-Band; MMIC; GaAs; radar; integrated circuit.

1. INTRODUCTION

Transmit/receive module (T/R module) is one of the most important elements in a radar system. A phased array antenna in a radar system uses thousands of such T/R modules. Figure 1 shows a block diagram of a T/R module. For the receiving function of T/R module, a low noise amplifier (LNA) is the key component that affects a lot of important system parameters such as noise figure (NF), gain, bandwidth (BW), spurious free dynamic range (SFDR), and spectral purity... The emerging in applications of radar systems, especially at X-band and Ku-band frequencies, necessitates wide frequency range, low noise, high gain, and high power T/R modules. Hence, a low noise, wideband, high gain, and high power LNA is highly demanded for next generation radar systems.

Recently, there are a lot of publications about X-band LNA. Some of them were designed on silicon substrate technology [1- 3]. This technology can provide good noise figure and frequency performance with small dimension factors. However, some other crucial components in T/R module, such as power amplifier and switch, need to be developed with higher power and reliability that the silicon substrate technology cannot achieve. Gallium Arsenide (GaAs) technology, on the other hand, can provide high reliability and higher power density. The ref. [4] presents a 8 to 10 GHz LNA on 0.25 µm GaAs pHEMT with an output P_{1dB} of 14 dBm. Besides, the LNA has a minimum noise figure of 1.4 dB and the gain of 29 dB. In [5], the monolithic

GaAs LNA achieves a very low noise figure of 0.5 dB and 30 dB gain. The frequency range of this LNA is, however, only from 7 to 10 GHz and the output P_{1dB} is 10 dBm.

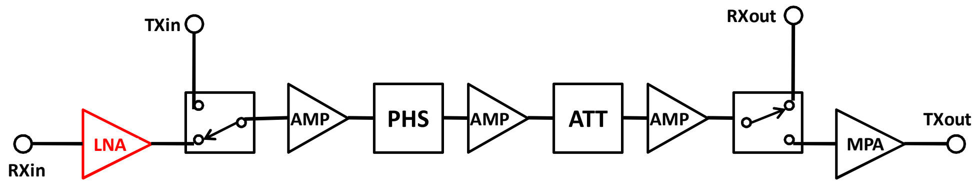

Figure 1. Block diagram of a T/R module.

This paper proposes a design of wideband, low noise, high gain, high power, and linearity monolithic LNA on 0.15 µm pHEMT technology. The LNA achieves a bandwidth of 6 to 12 GHz. In this operating frequency band, the proposed design has the minimum NF of 1.3 dB and over 25 dB small signal gain. The output 1 dB compression point is 16 dBm and the maximal third-order intercept point (OIP3) is 33 dBm.

2. CIRCUIT DESIGN AND TECHNOLOGY

2.1. Devices technology and characteristic

This LNA is designed on 0.15 µm double recess GaAs Pseudomorphic High Electron Mobility Transistors (pHEMT) process from Win Semiconductor [6]. This process is built on 100 µm GaAs substrate and demonstrates good device level performance with f_t of 90 GHz, power density of 860 mW/mm at 29 GHz, more than 10 dB gain per transistor and 50 % power added efficiency. The process exhibits high breakdown voltages of 16 V and therefore provides substantial operating margin for high reliability. It also allows a good minimum noise figure of about 0.5 dB at 10 GHz for the 2 ×75 µm gate width transistor.

2.2. LNA topology

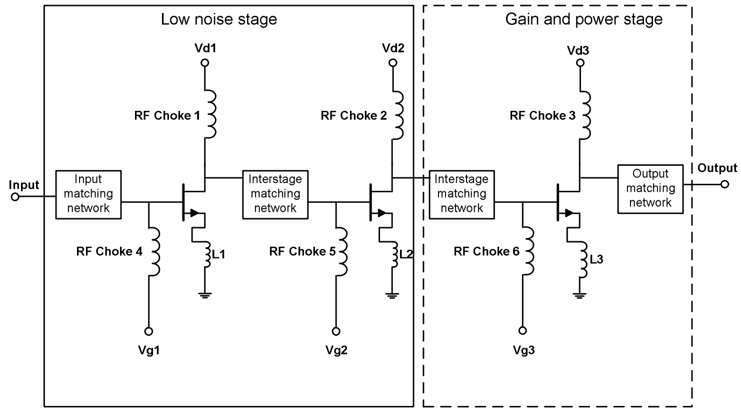

Figure 2. LNA topology.

Figure 2 shows the designed LNA topology. This LNA consists of three transistor stages in order to produce enough gain. The first two transistor stages are designed to have a low noise figure, whereas the last stage is optimized for gain, output power and stability. Choke inductors are used at all DC bias circuits to prevent radio frequency signal leakage. The LNA utilizes source degeneration matching technique with common source topology in order to achieve good return loss and low noise matching over a wide bandwidth simultaneously.

2.3. Design for low noise figure

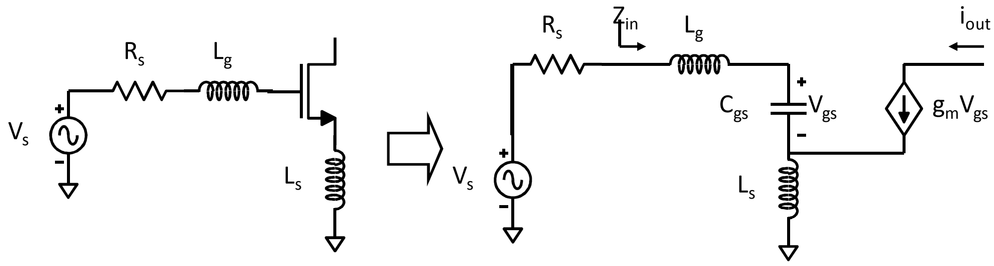

*Figure 3.*Inductive source degeneration topology and its small signal equivalent circuit.

As we mentioned in the previous section, the first two stages is matched for low noise figure. There are several matching techniques such as resistive termination, series-shunt feedback, input matched LNA (without degeneration inductor)... The first two techniques allow very good return loss. However, they are still noisy due to resistive noise source and attenuate signal. The input matched LNA technique delivers better noise figure matching but it's hard to achieve good return loss at the same time. In [7], good return loss and noise performance can be achieved simultaneously by using inductive degeneration technique which has topology shown in Figure 3. From its small signal equivalent circuit, the input impedance Z_{in} is calculated

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}}, \tag{1}$$

and the noise figure is

$$NF\big|_{\omega \approx \omega_0} = 1 + \gamma \frac{4(g_m L_s)^2}{R_s g_m} \frac{1}{C_{gs}(L_g + L_s)} = 1 + \frac{4\gamma L_s}{L_g + L_s} \tag{2}$$

where γ is empirical constant and equals 2/3 for long channel. (1) and (2) show that good return loss and noise matching can be obtained simultaneously by having large L_g and choosing appropriate L_s. Nevertheless, L_s should be selected carefully, because available gain is reduced with large L_s. In the first two stages of this design, the source degeneration inductor L_s is selected about 0.5 nH. [7] also states that a possible minimum noise factor for a device, F_{min}, is only achieved when a particular reflection coefficient, $\Gamma_s = \Gamma_{opt}$ is presented to the input

$$F = F_{\min} + \frac{4r_n \left|\Gamma_S - \Gamma_{opt}\right|^2}{\left(1 - \left|\Gamma_S\right|^2\right)\left(1 + \Gamma_{opt}\right)^2} \tag{3}$$

where F is the noise factor of a two port network; F_{min}, r_n, Γ_{opt} are noise parameters giving by the foundry or measured; Γ_s is the reflection coefficient at the input.

Therefore, after selecting L_s, the impedance of $\Gamma_s = \Gamma_{opt}$ is searched by doing source-pull simulation at the gate of transistor. For this design, the impedance of 120 + j145 Ω is found and the input matching network is optimized near this optimum noise matching impedance. The gate width of the transistors in the first and second stages is 150 µm. The transistors are biased at V_{d1} = V_{d2} = 2 V and V_{g1} = V_{g2} = -0.8 V with the drain current I_{d1} = I_{d2} = 22 mA.

2.4. Design of the third stage

Unlike the first two stages, the third stage of this LNA is designed for gain, output power and linearity. In order to have high output power and linearity, the bias point of this stage is moved to V_{d3} = 5 V and V_{g3} = -0.6 V for the drain current I_{d3} = 37 mA. The total gate width of this stage is also 150 µm. In this stage, a very small source degeneration inductor is used to enhance the stability of the whole circuit. Besides, this inductor also decreases third order inter-modulation distortion (IMD3) and helps to improve the linearity as discussed in [8]. The output-matching network is designed to balance between a good wideband S_{22}, flat gain and high output power.

3. THE LNA PROTOTYPE AND EXPERIMENTAL RESULTS

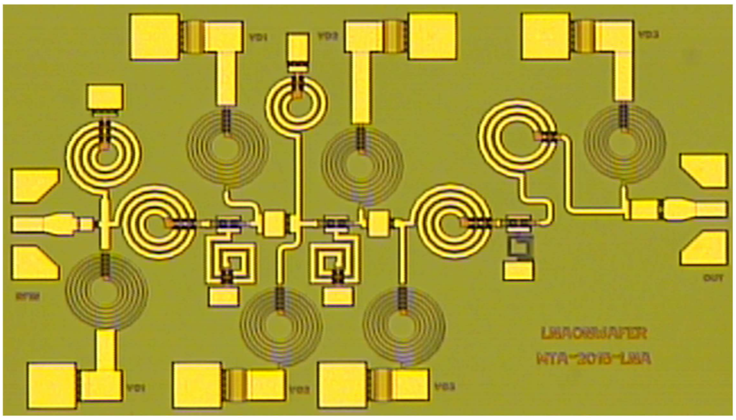

Figure 4. LNA chip photograph.

Figure 4 is the picture of the fabricated LNA chip. The dimension of the LNA die is 1.2 mm by 2.1 mm. At the LNA's input and output, ground-signal-ground (GSG) pads are placed for on-wafer measurement. Gate and drain of each transistor are connected to DC pads allowing to adjust bias point at each stage independently. At each DC pads, a small resistor and a bypass capacitor are attached to ensure for the stability and reliability. The coupling effects and parasitic of the layout are predicted by using electromagnetic simulator AXIEM of Microwave Office AWR [9]. As we can see in Figure 5, the measured small signal s-parameters of the LNA show that the operating frequency is from 6 to 11 GHz with over 25 dB small signal gain S_{21}. The input return loss S_{11} and output return loss S_{22} are better than 6 dB in this band. The measured noise figure over operating frequency range is illustrated in Figure 6. The LNA has the noise figure of about 1.3 - 2 dB for the frequencies from 5.7 to 12 GHz. Figure 7 shows the large signal simulation of the LNA at 10 GHz. From Figure 7, the P_{1dB} is at 16 dBm output power and -12.4 dBm input power. The OIP3 of this circuit is found by feeding 2-tones signal, which are separated by 10 MHz at the input. Figure 8 shows that the OIP3 is greater than 30 dBm from 8 to 12 GHz and has maximal OIP3 of 33 dBm at 10 GHz. Table 1 summarizes the performance of this design and compares with some previous published GaAs LNAs.

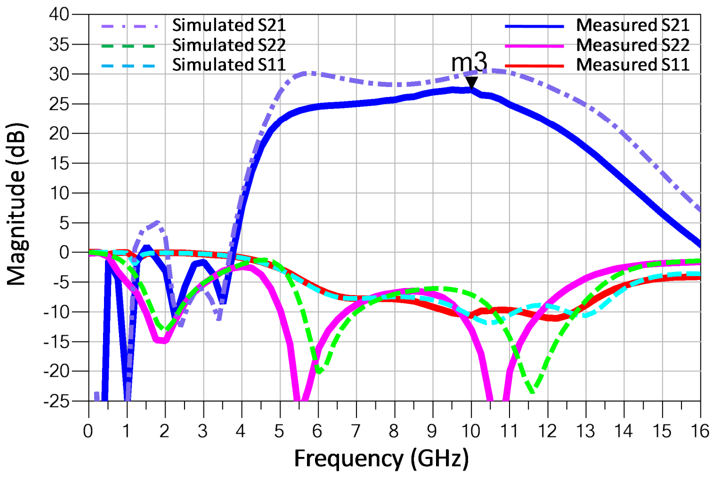

*Figure 5.*Simulatedand measured small signal s-parameters of LNA.

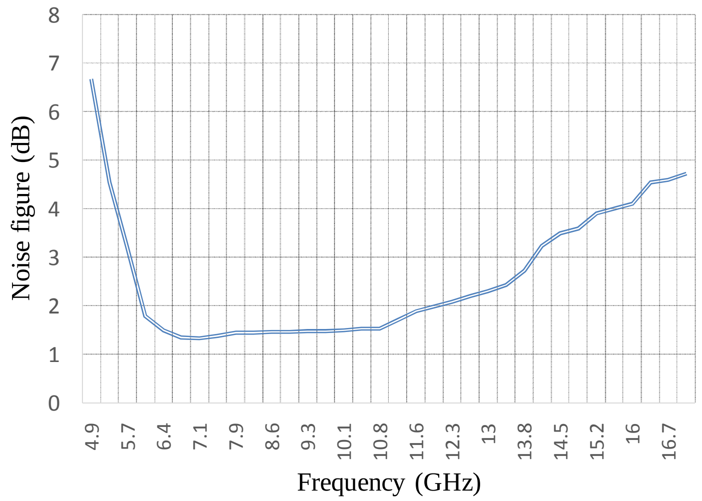

Figure 6. Measured noise figure.

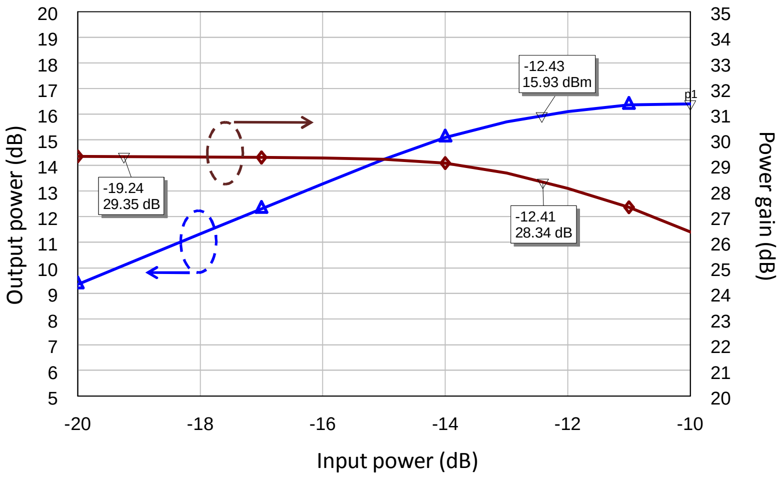

*Figure 7.*Output power versus Input power at 10 GHz.

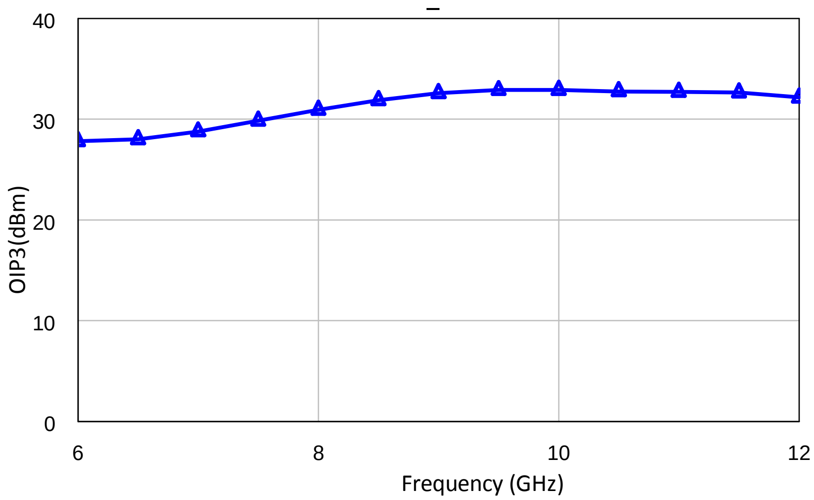

*Figure 8.*Output third-order intercept point versus frequency.

Table 1. LNAs comparison.

	Frequency (GHz)	Gain (dB)	P_{1dB} (dBm)	OIP3 (dBm)	NF (dB)	Chip Area (mm^2)	Process
[10]	6 - 14	20	12	24	1.3	2.05×1.2	GaAs
[11]	5 - 11	27	13	25	1.4	2.3× 1.35	GaAs
[12]	7 - 11	26	1	N/A	1	1.5× 1	GaAs
[13]	8 - 12	30	10	N/A	1.5	2.5× 1.5	GaAs
[14]	3.2-14.7	34	N/A	N/A	1.3	2.5× 1.5	GaAs
This work	6 - 11	25	16	33	1.3	2.1× 1.2	GaAs

4. CONCLUSIONS

A wideband X-band LNA integrated circuit have been designed using 0.15 µm GaAs pHEMT technology. In the frequency band from 6 to 11 GHz, the LNA achieves excellent performance with more than 25 dB gain and 1.3 - 2 dB noise figure. The output 1 dB compression power is 16 dBm and third-order intercept point is greater than 30 dBm. The LNA occupies 2.52 mm^2 and is unconditional stable.

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