DESIGN OPTIMIZATION OF EXTREMELY SHORT-CHANNEL GRADED SI/SIGE HETEROJUNCTION TUNNEL FIELD-EFFECT TRANSISTORS FOR LOW POWER APPLICATIONS

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ABSTRACT

This study investigates, by a two-dimensional simulation, the design optimization of a proposed 8 nm tunnel field-effect transistor (TFET) for low standby power (LSTP) applications utilizing graded Si/SiGe heterojunction with device parameters based on the ITRS specifications. The source Ge mole fraction should be designed approximately 0.8 because using lower Ge fractions causes severe short-channel effects while with higher values does not significantly improve the device performance but may create big difficulties in fabrication. Based on simultaneously optimizing the subthreshold swing, on- and off-currents, optimum values of source doping, drain doping and length of the proposed device are approximately 10^{20} cm^{-3}, 10^{18} cm^{-3}, and 10 nm, respectively. The 8 nm graded Si/SiGe TFET with optimized device parameters demonstrates high on-current of 360 μA/μm, low off-current of 0.5 pA/μm, low threshold voltage of 85 mV and very steep subthreshold swing of sub-10 mV/decade. The designed TFET with graded Si/SiGe heterojunction exhibits an excellent performance and makes it an attractive candidate for future LSTP technologies because of its reality to be fabricated with existing FET and SiGe growth techniques.

Keywords: graded Si/SiGe, low standby power (LSTP), short-channel device, tunnel field-effect transistor (TFET).

1. INTRODUCTION

Low power consumption is the leading goal in future integrated circuit (IC) technologies. For further reduction of power dissipation, IC devices are required to perform a steep on-off switching, i.e., a steep subthreshold swing (SS). While the SS of metal-oxide-semiconductor field-effect transistors (MOSFETs) is limited to 60 mV/decade at room temperature, tunnel field-effect transistors (TFETs), based on the band-to-band tunneling (BTBT), are not under this

limit [1, 3] and have been seen to be proper candidates for low power applications [4, 5]. A low off-current and low SS associated with a high on-current are the most important requirements of a TFET for low power ICs when scaling devices [6].

Although traditional material Si has been being quite successfully used in the semiconductor industry for a long time, the use of Si in TFET devices has been shown with low on-current that is not sufficient for low power ICs [3, 7, 8]. The BTBT current, which is a dominant gate-controlled current in TFETs, has been demonstrated to be strongly dependent on the semiconductor bandgap [9]. Therefore, it usually needs the tradeoff of the on- and off-currents in single material-based TFET devices [4, 8, 10, 11]. The on-current and the off-current in this kind of TFET exhibit as conflicting quantities under the impact of the bandgap. Another advantage of TFETs is probably its extensible scalability in continuing the Moore's law [1, 12]. Simulated tunneling generation shows that the tunneling active region is approximately 10 nm in Si-based TFETs so that tunnel transistors may be scaled down to 20 nm with only a slight increase in leakage current [1]. However, when the gate is scaled below this length, it leads to an exponential increase in off-current because of the direct source-to-drain tunneling [13] which is attributed to the present of lateral electric field on the full device length at any gate voltages [14].

In order to improve the device performance and further scale TFET devices, one has proposed a lot of techniques which can be roughly classified into two methods. The first method relates to modifying the structure of TFETs, such as double-gate [15], asymmetric structures [4], [16], ultra-thin body [11], gate-source/drain overlap/underlap [17, 18], and heteromaterial gate [19]. Alternative method concentrates on changing the material properties, such as low bandgap materials [4, 8], high-k gate dielectrics [15], and source/drain doping engineering [16, 20]. Among these techniques, an asymmetric structure of heterojunction is the most effective technique that is extremely helpful in overcoming the conflict between on- and off-currents to simultaneously achieve high on-current and low off-leakage [16]. A gate-oxide with high-k dielectrics can significantly boost the on-current, reduce the SS and extend the scalability [15], whereas the double-gate structure doubly improves the on-current [12]. Employing these techniques, a new graded Si/Ge heterojunction TFET has been recently proposed and numerically demonstrated its scalability into sub-10-nm regime with a record average SS of sub-10 mV/decade [21].

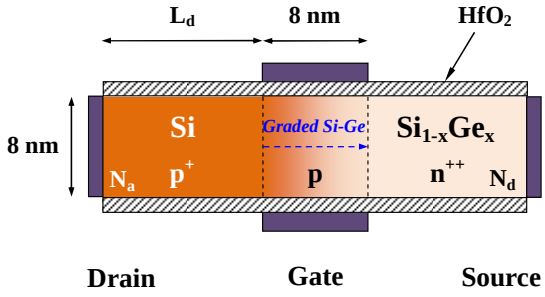

Figure 1. Schematic structure of a graded Si/SiGe heterojunction TFET with illustratively designed device parameters.

In this paper, a proposed extremely short-channel TFET with parameters based on the ITRS specifications of sub-10-nm technologies is meticulously investigated and optimally designed for LSTP applications using the graded $Si/Si_{1-x}Ge_x$ heterojunction. Simulator MEDICI [22] is

used to generate two-dimensional (2-D) simulations for designing the device. Section II describes the device structure, optimized parameters and simulation model while the design methodology is briefly stated in Section III. Section IV presents the design optimization of proposed TFET, and this optimized TFET is then compared to the ITRS roadmap in Section V which also essentially discusses the key fabrication process steps.

2. DEVICE STRUCTURE AND SIMULATION MODEL

The ITRS specifications for future technologies of 8-nm physical gate length are utilized to define the TFET structure. Fig. 1 shows the simulated structure of a p-i-n double-gate p-type TFET with asymmetric graded strained-SiGe/Si body whose thickness is taken to be 8 nm for satisfying the manufacturability [6], achieving low SS [15] and highest tunneling current density [23]. The drain region is defined as Si, and the source is specified by strained-$Si_{1-x}Ge_x$. For the p-channel region, the Ge mole fraction is linearly graded from x to zero when going from the source to the drain. High-k gate-dielectric HfO_3 with 3.8-nm thickness (EOT~0.7 nm) is defined at both gates of which a gate-workfunction of 5.1 eV is used, unless otherwise specified. The designed parameters, including source Ge fraction x, source doping N_d and its lateral gradient d (not shown in Fig. 1), drain length L_d and its doping N_a, are varied within reasonable ranges for the purpose of device optimization.

The operation of the TFET is analyzed by using 2-D device simulator MEDICI [22] in which the BTBT generation is calculated by the Kane's model [9] which has been experimentally validated in both Si- and SiGe-based tunnel devices [10, 24, 25] for a wide range of operating temperature [26]. In the Kane's model, the BTBT rate is formulated as:

$$G_{\mathrm{BTBT}} = A\frac{\xi^2}{E_g^{1/2}}\exp\left(-B\frac{E_g^{3/2}}{\xi}\right), \tag{1}$$

where E_g and ξ are the bandgap and electric field, respectively. Parameters A and B depend on the carrier effective mass m_e, the smaller m_e is, the higher is the BTBT current. The effect of small m_e in $Si_{1-x}Ge_x$ on the tunneling current is taken into account by modifying parameters A and B to be 2.24×10^{21} $(\mathrm{eV})^{1/2}/\mathrm{cmsV}^2$ and 15.7×10^6 $\mathrm{V/cm(eV)}^{3/2}$, respectively [20]. Eq. (1) shows that the BTBT generation depends explicitly on the bandgap and the electric field which is determined by the tunneling width. The quantum confinement effect is not taken into account in the simulations because of its relatively small effect in the body thicker than 5 nm [27]. Because the trap-assisted tunneling is determined by the trap density which varies from fabrication to fabrication, it is also excluded in all simulations.

Figure 2(a) plots the current-voltage characteristics of the TFET with graded Si/Ge heterojunction (pure Ge at the source) for illustrating its operation. A very steep SS with relatively high on-current and low off-current is observed, which is attributed to the abrupt transition of tunnel barrier under gate voltage [21]. To visually understand the operation of the device, Fig. 2(b) and 2(c) show the band diagrams along the channel at on- and off-states, respectively. In the off-state, the tunnel barrier is wide and high to prevent the BTBT of electrons from the drain to the source. For high source-to-gate voltages, the tunnel barrier is narrowed and lowered at the source junction so that the electrons in the channel valance band can easily tunnel through the forbidden gap, so the device is appropriately turned on.

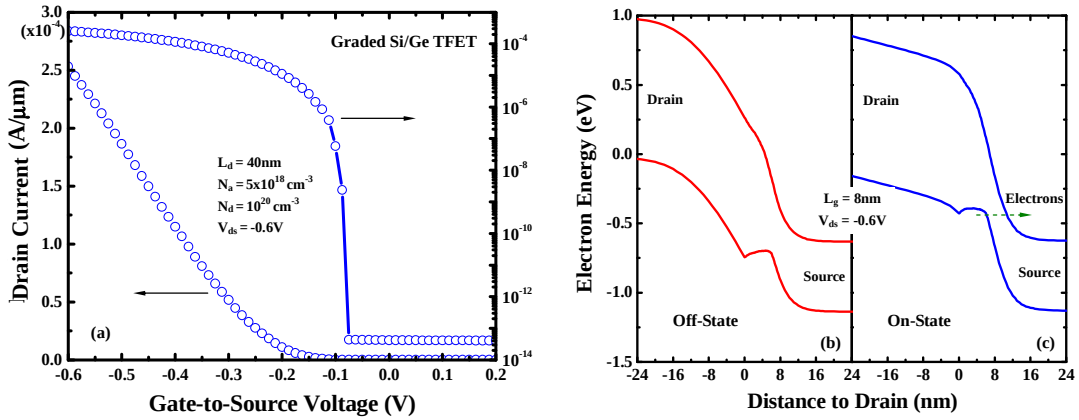

Figure 2. (a) Current-voltage curves, (b) off-state and (c) On-state energy-band diagrams, of 8 nm graded Si/Ge heterojunction TFET.

3. DESIGN METHODOLOGY

The operating characteristics of any SiGe-based TFETs rely highly on device parameters such as source/drain doping profiles [20, 28] and Ge concentration [2, 4, 10] which modifies the bandgap of Si-Ge alloy. Each parameter differently affects, in both manner and degree, the device performance. The source doping profile mainly affects the on-current and SS while the drain doping profile determines the ambipolar behavior [20]. Note that the same parameter may affect the device characteristics differently with different device structures [21, 29]. Furthermore, the fabrication process related to required parameters is also a very important issue not only to achieve the desirable device characteristics, but also to reduce the complication in fabrication for enhancing the IC reliability and cost.

Among the designed parameters, compositionally graded Ge concentration is the most important factor in graded SiGe TFETs because it affects not only the device performance through the bandgap engineering but also the quality of graded SiGe channel, which also crucially determines the performance of the device. A graded SiGe layer with high defect densities can severely degrade the device performance in subthreshold region by the trap-assisted tunneling [10, 30]. Therefore, the source Ge fraction is priority to be considered firstly. The source Ge concentration is chosen so that the role of bandgap engineering and the fabricability are balanced accordingly because higher Ge fractions improve the on-current but may also degrade the SS because of higher defect densities generated in fabrication processes. The design optimization of the source and the drain are then considered subsequently. In single material-based TFET, higher source doping and larger abruptness greatly improve the on-current and SS [20, 28]. Thereby, the effect of source doping profile is first investigated and optimized appropriately. For long-channel TFETs, the drain doping profile only influences the ambipolar leakages [20]. However, it may exacerbate short-channel effects (SCEs) in sub-10-nm TFETs because of the extreme proximity of the source and drain junctions [21]. Carefully considering the effect of drain, including both its length and doping concentration, is expected to further optimize the device performance. Acceptably chosen device parameters of both the source and the drain are based on optimization of the on-current, off-current and SS simultaneously.

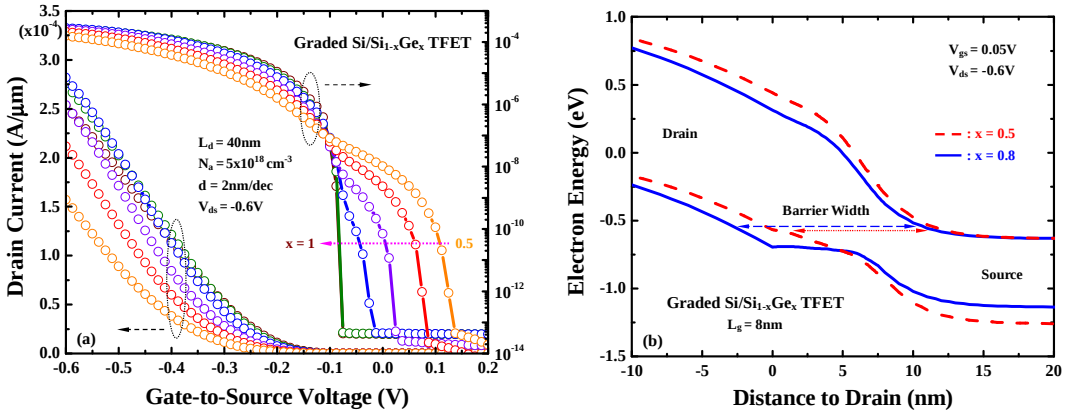

Figure 3. (a) Current-voltage curves and (b) off-state energy-band diagrams of 8-nm graded $Si/Si_{1-x}Ge_x$ heterojunction TFET with various source Ge fractions.

4. DESIGN OPTIMIATION

4.1. Ge mole fraction

To investigate the effect of Ge concentration on the performance of graded $Si/Si_{1-x}Ge_x$ TFETs, the Ge fraction x in the source is varied from 1 down to 0.5. Consequently, the abruptness of the graded heterojunction from the source to drain also decreases correspondingly. The source/drain doping profiles are kept at reasonable values and the drain length is fixed at 40 nm to definitely exclude its effect on the SCEs. To equitably compare the capability of how good switching is achieved, the gate workfunction is appropriately adjusted when changing the Ge fraction to generate the same threshold voltage which is commonly defined at the drain current of 0.1 μA/μm.

Figure 3(a) shows the current-voltage curves of 8-nm graded Si/SiGe TFET with various source Ge fractions. Excellent on-off switching with nearly ideal SS is demonstrated at high Ge fractions, whereas it is degraded at small compositions of Ge. The smaller Ge fraction is, the higher SS is observed. The increase of SS is attributed to the decrease of abruptness of the graded heterojunction. As shown in Fig. 3(b), highly abrupt junction by a high Ge fraction x = 0.8 results in relatively smooth transition of the channel energy-band to ensure a wide tunnel barrier for minimizing the tunnel leakage and an abrupt transition of the tunnel barriers for obtaining a steep SS [21]. Although the on-current does not suffer seriously from reducing the Ge fraction down to 0.5, the degradation of SS is a critical disadvantage in low power applications. The increase in SS raises the tradeoff between on-current and off-current when scaling the supply voltage. The price paid is a high leakage current when choosing a high on-current and vice versa. For a given supply voltage V_{dd} = 0.6 V, Fig. 3 shows that an acceptable Ge concentration at source is approximately 0.8 at which the SS is relatively small to suppress the appearing of the tradeoff of on- and off-currents.

Choosing a mild Ge concentration is further consolidated by considering growing processes of strained-SiGe on Si-substrate. Compositionally graded layers of strained-SiGe can be growth by either untra-high-vacuum chemical vapor deposition (UHVCVD) or molecular beam epitaxial (MBE) techniques [31]. Because the critical thickness of strained-SiGe layers on Si-

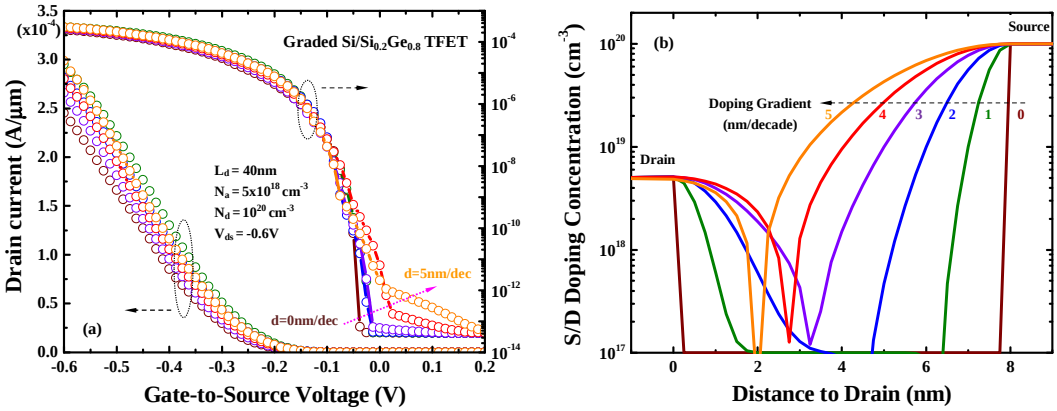

Figure 4. (a) Current-voltage curves and (b) doping profiles from source to drain of 8 nm graded $Si/Si_{0.2}Ge_{0.8}$ heterojunction TFET with different doping gradients.

substrate is exponentially reduced when rising Ge concentration [32], it is much more difficult to grow strained-SiGe layers with high Ge concentrations without developing defects. The defects severely degrade the device performance in subthreshold region because of the trap assisted tunneling [10, 30]. It has been theoretically and experimentally shown that the critical thickness of strained-SiGe layers are only about 1 nm for Ge concentrations higher than 0.8. Although strained-SiGe is grown with compositionally grading Ge concentration, which may mitigate the formation of dislocations, such very small critical layer thicknesses at high Ge concentrations may still cause high defect densities in strained-SiGe. So, to balance the effect of bandgap engineering and fabrication technology, a mild Ge concentration should be chosen to be around 0.8. With this source Ge concentration, it is expected to be possible to grow an 8-nm strained layer of compositionally graded SiGe without significant defects [16].

4.2. Source doping profile

As analyzed in previous subsection, henceforward, a source Ge mole fraction 0.8 is utilized in all simulated TFETs. It has been shown in long-channel TFETs that the source with as heavy doping and high abruptness as possible is expected to improve the on-current and SS [20, 28]. Because of a novel graded SiGe layer formed in the channel and the source and drain junctions are very close to each other in this proposed TFET, the effect of source doping profile may present differently, and therefore the role of source must be investigated in detail.

Figure 4 shows the current-voltage curves of the graded $Si/Si_{0.2}Ge_{0.8}$ TFET with various source/drain doping gradients. The device characteristics of the TFET only slightly changes under increase of the gradient up to 5 nm/decade which is comparable to the channel length. This property allows more flexibility in the design of device. To investigate the effect of source doping on the device characteristics, a reasonable doping gradient of 2 nm/decade is used for both source and drain junctions. As shown in Fig. 5(a), a source doping N_d approximately 10^{20} cm^{-3} is preferable to optimize both the on-current and the SS. A lower source doping considerably degrades the on-current because of wider tunnel barrier [20], whereas higher values seriously degrade the SS and on-state current. The lowering of on-current when increasing the source doping above 10^{20} cm^{-3} is attributed to the increase of tunneling barrier height because of the shift of tunneling location far from the source junction. To understand this different effect on the SS from conventional long-channel TFETs, Fig. 5(b) plots the energy-band diagrams with

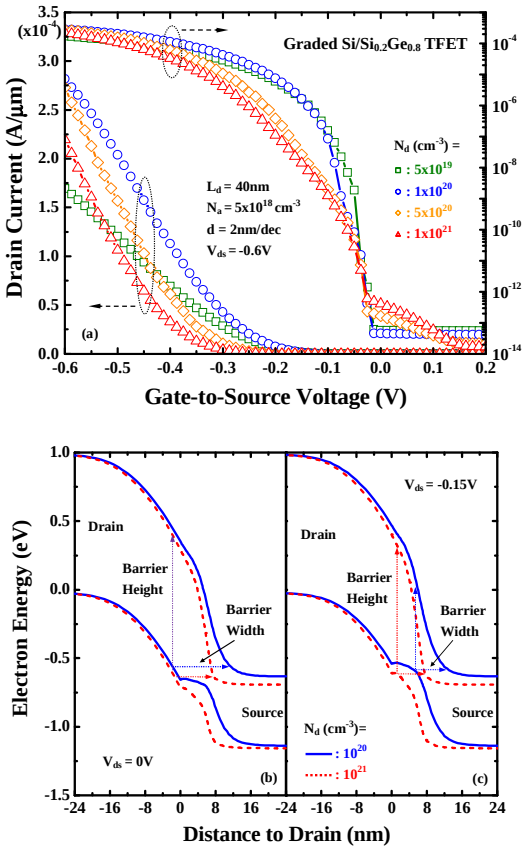

Figure 5. (a) current-voltage curves and (b) energy-band diagrams of 8-nm graded Si/$Si_{0.2}Ge_{0.8}$ heterojunction TFET with different source doping concentrations.

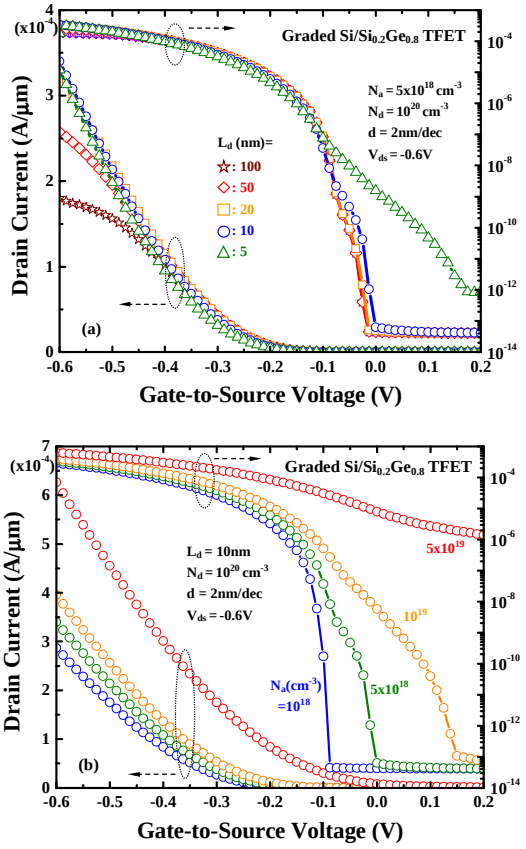

Figure 6. Current-voltage curves of 8-nm graded Si/$Si_{0.2}Ge_{0.8}$ heterojunction TFET with different (a) drain lengths and (b) drain doping copncentrations.

two different doping values in the subthreshold condition. At V_{gs} = 0 V (left panel), a heavier source results a narrower tunnel barrier, so the off-state leakage is higher. For V_{gs} = -0.15 V (right panel), however, the tunneling barrier height of 10^{21} cm^{-3} source TFET is considerably higher than that of 10^{20} cm^{-3} source, which results a lower tunneling current. These properties, which originate in the graded Si/SiGe, clearly explain the degradation of SS in the extremely heavy source TFETs.

4.3. Drain engineering

It is shown that the ambipolar leakage current in TFET devices at off-state regimes originates from the tunneling of carriers in the drain-side junction [11, 12]. Therefore, the drain tunneling junction should be appropriately engineered to suppress the tunneling leakage. The decrease in drain doping makes a significant decrease in the ambipolar current [20]. For extremely short-channel TFETs, both the drain length and doping may considerably affect the SCEs. Because these effects are sensitive to the channel length and the extraordinary structure of graded Si/SiGe, a detail investigation is necessary for further understanding and improving the TFET characteristics.

Figure 6 shows the current-voltage curves of 8 nm graded Si/$Si_{0.2}Ge_{0.8}$ TFETs with various

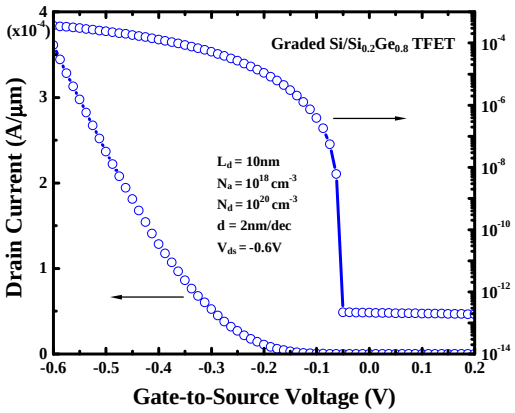

Figure 7. Current-voltage characteristic of an optimized 8 nm graded $Si/Si_{0.2}Ge_{0.8}$ heterojunction TFET.

drain lengths L_d and doping concentrations N_a. The drain doping is fixed at a medium value when varying the drain length, whereas the optimized drain length is utilized when changing the drain doping. Generally, the on-current is further enhanced by the shorter drain length and higher doping, which make decreasing the drain resistance. As seen in Fig. 6(a), a too long drain causes a significant decrease in the on-current, and a too short drain (shorter 10 nm) also results in severe SCEs. To achieve high on-state current, steep SS and highly scaled TFET, the drain length should be designed down to approximately 10 nm. With the drain length fixed at 10 nm, it is shown in Fig. 6(b) that a heavy drain seriously degrades the SS by severe SCEs. Although the on-current is little higher in case of $5x10^{18}$ cm^{-3} TFET compared with this of 10^{18} cm^{-3}, its considerably higher SS makes it not competitive in the view point of which all the SS, drive current and off-leakage leakage should be simultaneously optimized. Indeed, with the significantly smaller SS, the current-voltage curve of 10^{18} cm^{-3} can be further engineered by the gate workfunction to achieve a higher on-current while still keeping the same off-state leakage. Selecting a relatively low drain doping of 10^{18} cm^{-3} with an extremely short length is an optimal design to not only retain low drain resistance but also scale the total size of device further.

5. OPTIMIZED TFET VERSUS ITRS ROADMAP

In order to evaluate the possibility of proposed device as a potential candidate for low power applications, the proposed graded Si/SiGe TFET with optimized parameters is compared to key ITRS requirements of low standby power devices for 2023 node. Fig. 7 shows the current-voltage curves in linear and logarithmic scales of an optimized 8-nm graded $Si/Si_{0.2}Ge_{0.8}$ heterojunction TFET. The designed device presents a very steep SS, relatively high on-current and low off-state leakage. For more details, Table I summaries main device parameters and characteristics of the designed TFET, the ITRS specifications and the $Si_{0.8}Ge_{0.2}$-source TFET in Ref. [4] for further comparison. The proposed TFET meets all basic ITRS requirements for the 2023 LSTP technology. As compared to Ref. [4], this work presents a significantly higher on-current, lower SS although the channel length is extremely scaled and the equivalent oxide thickness is also relatively thicker. The steep SS is attributed to the abrupt transition of tunnel barriers while the high on-current is due to the low-bandgap of strained-$Si_{0.2}Ge_{0.8}$ [21].

Finally, it is believed that such a graded Si/SiGe structure of designed TFET can be performed by planar or vertical 3-D architectures. To take a planar double-gate structure as an

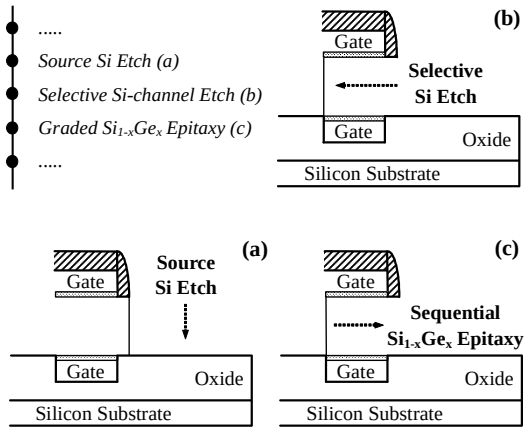

Figure 8. Key process steps and schematic sketches of a feasible device structure for proposed TFET with a graded Si/SiGe heterojunction.

Table 1. Designed device parameters and characteristics in comparison with the ITRS specifications.

ITRS Requirements for 2023 LSTP Technology		This work	Ref. [5]
Physical Gate Length (nm)	8.2	8	53
Body Thickness (nm)	5	8	10
Doping Gradient (nm/dec)	1.8	2	2~3
EOT (nm)	0.71	0.7	0.56
Power Supply (V)	0.61	0.6	1.2
Threshold Voltage (mV)	485	82	280
Drive Current (μA/μm)	248*	360	200
Leakage Current (pA/μm)	10	0.3	0.001
Subthreshold Swing (mV/dec)	-	5	12.3

** Drive current for p-type is assumed to be 50% of n-type MOSFET*

example, Fig. 8 shows key steps and schematic sketches of a proposed feasible process which employs existing planar process flows of conventional MOSFETs [33]. Additional key processes in the fabrication of proposed graded Si/SiGe TFET are successionally implemented by selectively etching Si-channel and then growing $Si_{1-x}Ge_x$ epitaxial layer with Ge concentration increased from the drain (pure Si) to the source (~80 % Ge). The graded $Si_{1-x}Ge_x$ is compressively strained because of its ultra-thin layer [32] and this strain is helpful in improving the tunneling current by considerably decreased bandgap [10, 16, 27]. The most challenge of fabricating such a graded TFET is to form a high quality graded $Si_{1-x}Ge_x$ layer with as low defect density as possible to suppress the trap-assisted tunneling which may degrade the SS. Because the generation of defects in strained-$Si_{1-x}Ge_x$ is extremely sensitive to the temperature, low temperature processes are preferred to attain a low defect density. The Ge concentration is the key parameter and has to be exactly controlled to achieve favorably predicted characteristics of the graded $Si/Si_{0.2}Ge_{0.8}$ TFET.

6. CONCLUSIONS

A 2-D simulation has been demonstrated to investigate the design optimization of an extremely short-channel TFET proposed with a novel graded Si/SiGe heterojunction. The Ge mole fraction at the source is chosen by trading-off between the bandgap engineering and fabrication technology. The source doping profile differently affects the device characteristics in extremely scaled graded Si/SiGe TFET so that a reasonably high doping is preferable. A relatively lightly-doped and short drain should be designed to simultaneously suppress the short-channel effects, improve the drive current and achieve an extremely scaled device. With favorably enhanced performance compared to existing SiGe-based TFETs, the proposed TFET is highly promising for LSTP applications.

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TÓM TẮT

THIẾT KẾ TỐI ƯU BÓNG BÁN DẪN XUYÊN HẦM SỬ DỤNG CHUYỂN TIẾP DỊ CHẤT LIÊN TỤC SI/SIGE CHO ỨNG DỤNG CÔNG SUẤT THẤP

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Sử dụng mô phỏng hai chiều, nghiên cứu khảo sát thiết kế tối ưu của bóng bán dẫn xuyên hầm (tunnel field-effect transistor) 8 nm sử dụng chuyển tiếp dị chất liên tục Si/SiGe cho các ứng dụng công suất thấp (low power applications). Các tham số linh kiện được thiết kế phù hợp với chỉ dẫn quốc tế về công nghệ bán dẫn (international technology roadmap of semiconductors). Nghiên cứu chỉ ra rằng nồng độ Ge sử dụng ở cực nguồn (source) nên khoảng 0,8 vì nếu sử dụng nồng độ thấp hơn sẽ gây ra hiệu ứng ngắn kênh (short-channel effect) nghiêm trọng trong khi nếu dùng cao hơn cũng sẽ không cải tiến đáng kể mà còn gặp nhiều khó khăn trong việc chế tạo. Dựa trên việc tối ưu đồng thời độ dốc dưới ngưỡng (subthreshold swing), dòng dẫn (on-current) và dòng rò (off-current), các giá trị tối ưu của nồng độ cực nguồn, nồng độ và chiều dài cực máng (drain) cho bóng bán dẫn xuyên hầm được đề suất lần lượt là 10^{20} cm^{-3}, 10^{18} cm^{-3}, and 10 nm. Sau khi được tối ưu hóa, bóng bán dẫn xuyên hầm 8 nm sử dụng chuyển tiếp dị chất liên tục Si/SiGe đã chứng tỏ dòng dẫn cao khoảng 360 μA/μm, dòng rò thấp cỡ 0,5 pA/μm, hiệu điện thế ngưỡng thấp 85 mV và độ dốc dưới ngưỡng thấp dưới 10 mV/decade. Bóng bán dẫn xuyên hầm được thiết kế sử dụng chuyển tiếp dị chất liên tục Si/SiGe cho thấy hoạt động rất tốt và vì vậy có thể là một linh kiện tiềm năng cho công nghệ bán dẫn công suất thấp trong tương lai vì việc chế tạo là khả thi với công nghệ bóng bán dẫn và kĩ thuật cấy lớp SiGe hiện có.

Từ khoá: Si/SiGe, công suất chờ bé, linh kiện kênh ngắn, transito trường xuyên ngầm.