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NEW PWM SWITCHING TECHNIQUES FOR AN OPTIMUM CASCADE 3/3 NPC INVERTER OPERATION

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Tóm tắt. Các nghiên cứu và ứng dụng trong công nghiệp đã chứng tỏ những đặc điểm nổi bật của biến tần đa bậc bao gồm: chất lượng công suất lớn, hài thấp, nhiễu điện từ thấp, và tổn hao đóng ngắt thấp. Trong những năm gần đây, một số mô hình biến tần lai được phát triển nhằm tăng chất lượng điều khiển và giảm độ phức tạp trong điều khiển cho biến tần. Trong số đó, thông qua kết nối nối tiếp của 2 bộ biến tần NPC ba bậc, bộ biến tần lai 3/3 NPC được hình thành với nhiều ưu điểm vượt trội. Bài báo trình bày những kỹ thuật PWM mới dựa theo phương pháp sóng mang nhằm điều khiển vận hành tối ưu cho mô hình ghép này. Về mặt nguồn DC, cấu trúc biến tần này được cấp nguồn theo cấu trúc nguồn chung (với chỉ một nguồn DC) hay cấu trúc nguồn riêng với 4 nguồn DC (là các pin mặt trời). Các mô phỏng và thực nghiệm trong bài báo sẽ được thực hiện để kiểm tra và đánh giá các kỹ thuật được đề xuất.

Abstract. Investigations and industrial applications have demonstrated unique and attractive features of multilevel inverters including high power quality, good harmonic performance, good electromagnetic compatibility, and low switching losses. In recent years, several new cascaded multilevel inverters are developed for increasing drive performance, reducing the drive complexity and losses. Among those, through a series connection of two three-level NPC inverters, a cascade-3/3 inverter is created with enormous advantages. This paper presents new carrier-based PWM modulations to control this dual topology for optimum operation. In terms of power sources, this cascaded inverter is operated either from isolated dc sources (series power cells) or from a single dc source. Computational simulation and experimental validation are given to verify the proposed techniques.

1. INTRODUCTION

This paper presents carrier based PWM techniques for the cascaded diode-clamped inverter as shown in figure 1, where two three-level NPC inverters are series connected by splitting the neutral point of the load. This cascade-3/3 system has many advantages over fundamental multilevel topologies alone for medium-voltage applications including:

• High power quality with a relatively low number of semiconductors due to the compounding effect of the voltage levels.

• Redundant switching states (both joint-phase redundancy and per-phase redundancy) providing some flexibility in the multilevel inverter modulation to achieve certain control objectives.

• Feasible operation from only one dc source available or from isolated dc sources which are

the series connections of power cells.

• The reliability of this system in which the dual nature of the inverter could be used to drive the motor in fault situations through systems re-configuration.

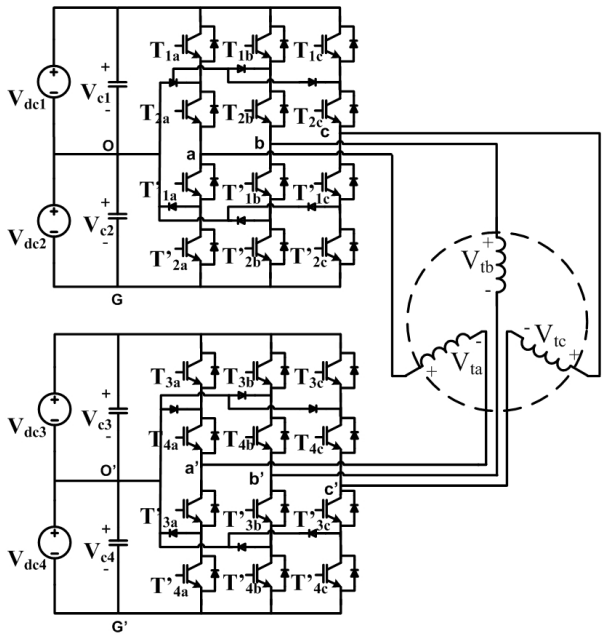


Figure 1. The cascade-3/3 multi-level inverter

Recent development in the control methods of this topology has witnessed two main trends. The first advance was an attempt to increase the number voltage levels of the cascaded inverter by supplying two three-level inverters from unequal voltage sources to reach maximum distention operation [1] or modulating the inverter in over-distention operation in spite of some missing switching levels [2]. The second advance was that the redundant switching states (RSS) were selected properly in order to control the cascade-3/3 topology from a single dc voltage source for Naval ship propulsion [3].

In this paper, two three-level inverters are operated from dc sources with equal voltages; therefore, the resulting inverter could emulate a five-level inverter. Meanwhile, several novel carrier PWM approaches are proposed to accomplish certain goals such as obtaining output commanded voltages with controllable amplitude and frequency, decreasing switching losses through the utilization of switching redundancy within a phase, reducing total harmonic distortion (THD) by minimizing output voltage ripple, and balancing the switching intensity of each IGBT in the topology for sustainable operation.

2. CASCADE 3/3 INVERTER TOPOLOGY

Figure 1 shows the topology of a cascade-3/3 motor drive. Therein, the dual inverter with equal dc sources fed by photovoltaic cells or passive rectifiers is structured into two kinds of

connection with a single DC source or isolated dc sources. This inverter consists of 24 IGBTs which are switched based on general rules as

$$\begin{cases} T_{ij} + T'_{ij} = 1, \\ \\ T_{ij} \geq T_{ij+1}, \end{cases} \qquad (1)$$

where switching states T_{ij} and T'_{ij} with $i = a, b, c$ defined for the $a - b-$ and $c-$phase, respectively, and $j = 1, 2, 3, 4$. In figure 1, since the transistors are always switched in pairs, the complement transistors are labeled T_{ij} and T'_{ij} accordingly. Each phase a, b, and c can be connected to any DC bus in the capacitor bank by gating switching transistors T_{ij} and T'_{ij} off (off = 0) or on (on=1). From a system point of view, if both three-level inverters are supplied from isolated dc sources with equal voltages $V_{c1} = V_{c2} = V_{c3} = V_{c4} = V_d$, then the inverter topology can be replaced correspondingly by a simple model in figure 2.

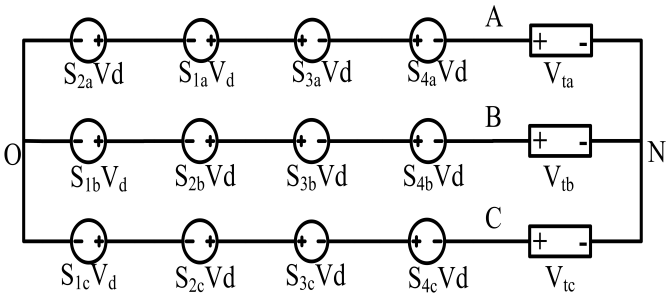


Figure 2. Corresponding model of the cascaded inverter

This model is derived from a split of loads at the end of one three-level inverter to create a new load neutral point. The distinguishing between DC sources and three-phase loads brings about more straightforward analysis and modulation for the cascaded topology.
Based on the corresponding model, inverter output line-to-ground voltages (defined from the phase nodes A, B and C to the negative rail of the dc bus) can be directly controlled through the switching states using KVL equation as

$$V_{IO} = (T_{i1} + T_{i2} - T_{i3} - T_{i4}). \qquad (2)$$

In Table 1, there are several switching state combinations yielding the same output line-to-ground voltages. This advantageous characteristic referred to as per-phase RSS (Redundant Switching Selection) offers the high efficiency in switch utilization.

Table 1. The relationships between per-phase switching state sequences and line-to-ground voltages

V_{IO}	(T_{i1},T_{i2},T_{i3},T_{i4})
-2Vd	(0,0,1,1)
-Vd	(0, 0, 1, 0); (1, 0, 1, 1)
0	(0, 0, 0, 0); (1, 1, 1, 1); (1, 0, 1, 0)
Vd	(1, 0, 0, 0); (1, 1, 1, 0)
2Vd	(1, 1, 0, 0)

A variety of redundant states can be selected for particular switching algorithms to boost the qualification of output voltage such as reducing switching losses and output-voltage ripples. In other applications as [3] and [4], per-phase RSS along with joint-phase RSS is used to meet certain goals in capacitor's balance or over-distention operation.

3. PRINCIPLE OF OPERATION

In general sine-triangle modulations, modulating signals are compared with $n-1$ triangle waveforms (n is defined as the number voltage levels of inverter) to create respective PWM control. In this section, a simple and flexible carrier based PWM method in time domain is used to implement all proposed modulations in later sections.//

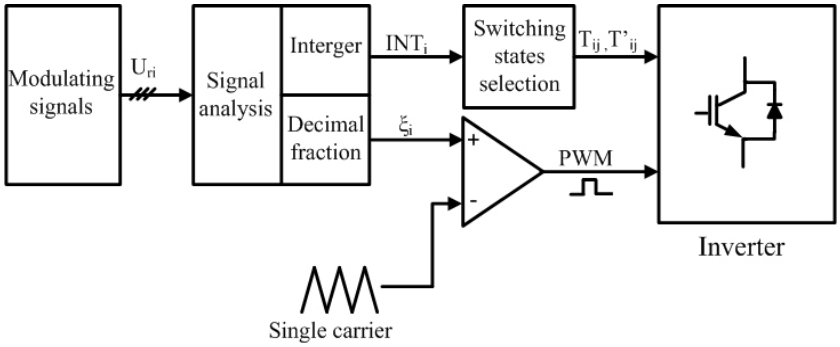


Figure 3. Carrier based PWM scheme

In figure 3, the modulating signals, instead of directly compared with $n-1$ carriers, are broken down into two components including INT_i, the nearest lower voltage levels and ξ_i, switching time signals. In this formula, INT_i defined as matter of integerizing the modulating signals is employed to schedule the transistors' switching during the switching period, and the reference signals ξ_i which is a decimal fraction of U_{ri} represents the information of amplitude and phase of modulating signal involved in a level unit; therefore, this component can be used to calculate the dwell time of transistors:

$$U_{ri} = INT_i + \xi_i. \qquad (3)$$

In this modulation, in order to reduce complexity in processing algorithm, a dc offset is added to the U_ri to regulate the modulating signals positive. In this sense, if the intergerizing part of the a-phase duty cycle (or modulating signal), for example, is updated as INT_i, then the states in this table respective to output voltage levels of $(INT_i - 2)\,Vd$ and $(INT_i - 1)\,Vd$ are used to control transistors switching. Obviously, the INT_i component maintains an important role to determine the commanded level of output voltage. Meanwhile, switching time signals ξ_i, another component of the duty cycle, is compared with reference carrier in figure 4 (the formula (4)) to create pulse-width modulation. The role of this part is to ensure the output voltage shape similar to the commanded voltage.

$$T_i = \begin{cases} 0 & C_i \geq \xi_i \\ 1 & \text{elsewise} \end{cases} \qquad (4)$$

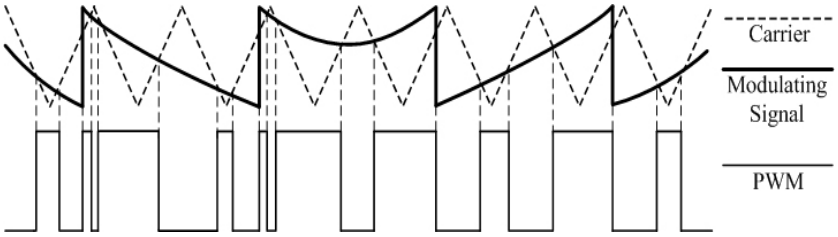


Figure 4. Pulse Width Modulation of carrier based methode

In space vector modulation, since dc offset component is included in the two-dimensional voltage vector plot, the output voltage space vector tracks an ideal circle with the maximal modulation index m = 0.866. By contrast, in switching frequency optimal (SFO) modulation of carrier-based method, a dc offset needs to be added to the modulating signals to obtain discontinuous waveforms for optimizing switching harmonics as well as increasing the maximum amplitude of output voltage. The modified modulating signal is calculated as

$$U'_{ri} = U_{ri} + V_{offset}, \tag{5}$$

where, Voffset is related to the modulating signals by

$$\begin{aligned} V_{offset} &= \frac{V_{omax} + V_{omin}}{2}, \\ V_{omax} &= \frac{n-1}{2} - max(U_{ra}, U_{rb}, U_{rc}), \\ V_{omin} &= -\frac{n-1}{2} - min(U_{ra}, U_{rb}, U_{rc}), \end{aligned} \tag{6}$$

where n represents the number of voltage levels; V_{omax} and V_{omin} are determined from the maximum and minimum of the modulating signals

4. PROPOSED MODULATION METHODS

4.1 Switching frequency reduction

As presented in the previous section, the special topology offers redundancy in choosing different switching states making up the same output voltage level. In this section, a use of RSS is reduction in the commutation of transistor's switches for improvement in drive efficiency. The process involves considering the present transistor switching states and the redundant choices for the next states. The choice can be made based on the states that result in the least number of transistor switches.

In the Table 2, there are 6 switching state patterns which are applied for switching frequency reduction. For instance, the third patterns with switching state sequences in turns is $(0,0,1,1) \rightarrow (0,0,1,0) \rightarrow (1,0,1,0) \rightarrow (1,1,1,0) \rightarrow (1,1,0,0)$. Manifestly, since the transitions between different voltage levels occur such as the transition from –2Vd to –Vd (it means that two chosen switching states are (0,0,1,1) and (0,0,1,0)), only one complement pair

of transistors among 12 ones is switching.

Table 2. Switching state sequences for switching frequency reduction

Patterns	VAO, VBO, VCO : $-2Vd \rightarrow -Vd \rightarrow 0 \rightarrow Vd \rightarrow 2Vd$
1	$(0,0,1,1) \rightarrow (0,0,1,0) \rightarrow (0,0,0,0) \rightarrow (1,0,0,0) \rightarrow (1,1,0,0)$
2	$(0,0,1,1) \rightarrow (0,0,1,0) \rightarrow (1,0,1,0) \rightarrow (1,0,0,0) \rightarrow (1,1,0,0)$
3	$(0,0,1,1) \rightarrow (0,0,1,0) \rightarrow (1,0,1,0) \rightarrow (1,1,1,0) \rightarrow (1,1,0,0)$
4	$(0,0,1,1) \rightarrow (1,0,1,1) \rightarrow (1,1,1,1) \rightarrow (1,1,1,0) \rightarrow (1,1,0,0)$
5	$(0,0,1,1) \rightarrow (1,0,1,1) \rightarrow (1,0,1,0) \rightarrow (1,0,0,0) \rightarrow (1,1,0,0)$
6	$(0,0,1,1) \rightarrow (1,0,1,1) \rightarrow (1,0,1,0) \rightarrow (1,1,1,0) \rightarrow (1,1,0,0)$

In the algorithm of this modulation, the state selection can be done off-line and programmed into an RSS table based on the level component INT_i.

4.2. Voltage ripple elimination

Following the switching frequency reduction, a vital algorithm to minimize voltage ripple in this paper is also implemented based on switching state redundancy. Herein, the switching transistors are utilized particularly so that output voltage transitions within $a-, b-$ and $c-$phase between different levels are of the same manners. For example, figure 5b) shows that while $a-$phase voltage level goes up from 0 to $Vd = 100V, b-$ and $c-$phase voltage level also increases from $\breve{}Vd = -100V$ to 0. Generally, these changes in distinctive levels of three-phase output voltages in a half of carrier period are similarly complied with either increasing or decreasing rules in comparison to unregulated transitions in figure 5a).

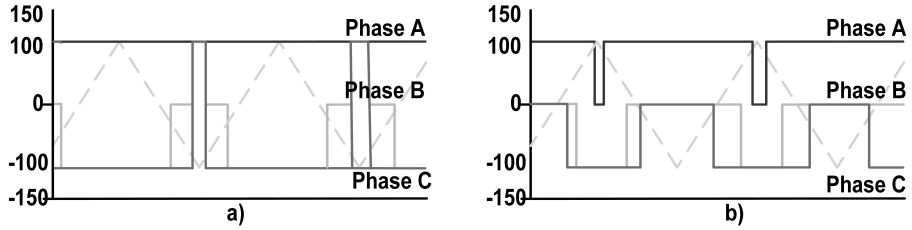


Figure 5. a),b)PWM after and before using proposed modulation

In space vector modulation, this algorithm is exactly equivalent to the selection of the three nearest vectors to create the commanded voltage vector. Thus, this provides less voltage deviation leading to the output near sinusoidal current with lower switching harmonics.
The algorithm of this modulation also opts for switching state sequences based on INT_i value; however, there are one or more arbitrary switchings of some states occurring at the end of new voltage transitions. Switching sequences in figure 6 and 7 can be used to exemplify the concept of operation. Therein, all transistors S_{ij} are off or on simultaneously at the end of the moment when output voltage transits from negative value to positive value or vice versa.
There is a note in the implement for this modulation. Even though the switching frequency is reduced remarkably, the even distribution of switching among transistors should be concerned. For example, in figure 6, it can be seen that only T_3, T_4 and their complement transistors are

switching constantly. In some proposed algorithm, both increasing switching sequences and decreasing switching sequences are coordinated to decentralize the switching density on any transistor.

V_{AO}, V_{BO}, V_{CO}	$(T_{i1}, T_{i2}, T_{i3}, T_{i4})$
−2Vd	(0, 0, 1, 1)
−Vd	(0, 0, 1, 0); (1, 0, 1, 1)
0	(0, 0, 0, 0); (1, 1, 1, 1); (1, 0, 1, 0)
Vd	(1, 0, 0, 0); (1, 1, 1, 0)
2Vd	(1, 1, 0, 0)

Figure 6. Decreasing switching transistor sequences

V_{AO}, V_{BO}, V_{CO}	$(T_{i1}, T_{i2}, T_{i3}, T_{i4})$
−2Vd	(0, 0, 1, 1)
−Vd	(0, 0, 1, 0); (1, 0, 1, 1)
0	(0, 0, 0, 0); (1, 1, 1, 1); (1, 0, 1, 0)
Vd	(1, 0, 0, 0); (1, 1, 1, 0)
2Vd	(1, 1, 0, 0)

Figure 7. Increasing switching transistor sequences

5. SIMULATION AND EXPERIMENTAL RESULTS

A computer simulation of this dual inverter in figure 8 is carried out using Power System blockset and Simulink blockset of Matlab software to demonstrate all carrier based modulations. In parallel, a laboratory prototype (figure 9 and 10) has been developed for verifying the cascade 3/3 five-level inverter's operation in practice. A 3-phase passive R-L load with $R = 16Ohms, L = 90mH$ is used for all simulations or experiments. Both simulation and experimental results are compared to illustrate the validity of cascaded inverter control.

5.1. Simulation and experiment results with different modulation index

Figures 11 and 12 show the multi-level inverter performance for various numbers of modulation index. The inverter was controlled with a fundamental component of fo $= 60hz, Vdc = 30V and fs = 5kHz$.

By observing the output currents and its FFT analysis in figure 11, it can be seen that since the two three-level inverters are supplied from a single dc voltage, the output current disturbance is represented by a third harmonic component. This can be explained by the fact that the connections between dc buses and two three-level inverters result in the correspondence of the dual inverter to a three-phase four-wire system. Therein, a leakage current exits and flows through load's and source's neutral points. Hence, that the extra current is added to phase

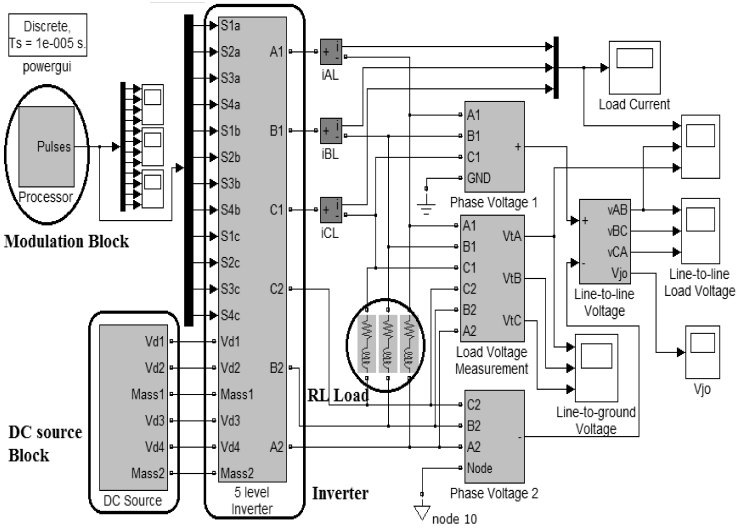


Figure 8. Simulation block of cascaded inverter system

current triggers the third harmonic. However, it is worth noting that the third harmonic to fundamental amplitude ratio is relatively small and can be tolerable in some applications such as controlling a high power motor. Although this tradeoff exists, a dispensable feature of this structure is used in case of a limited number of sources.

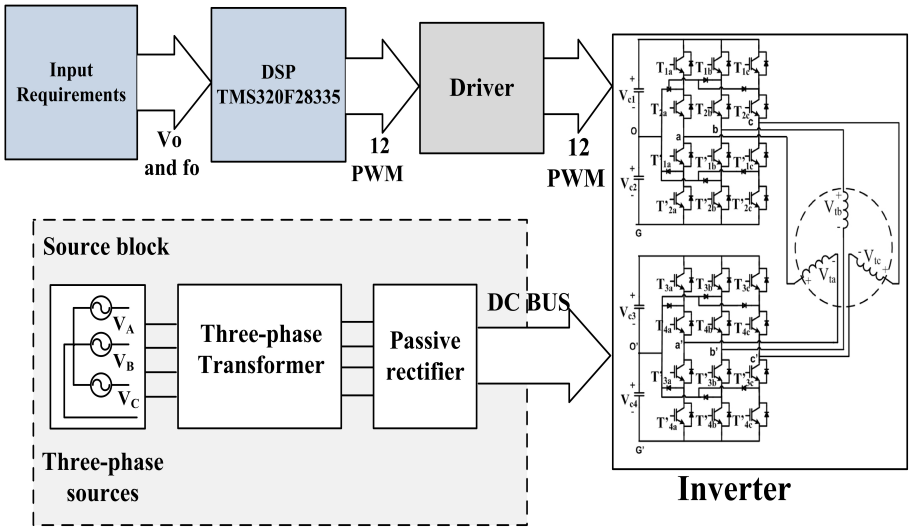
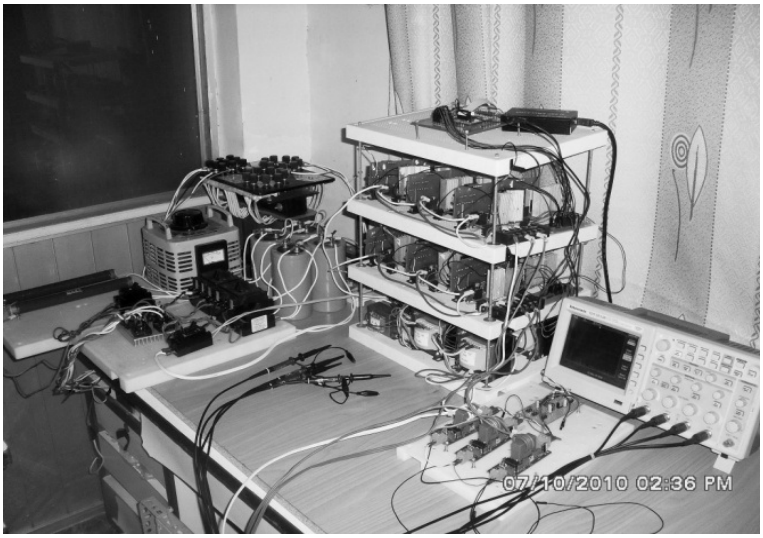
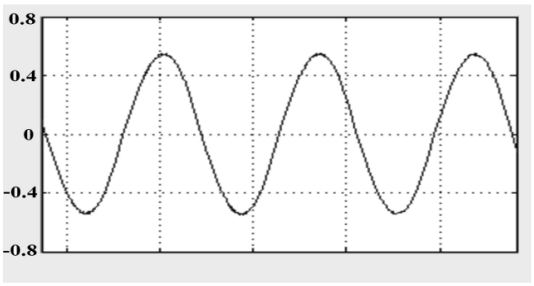


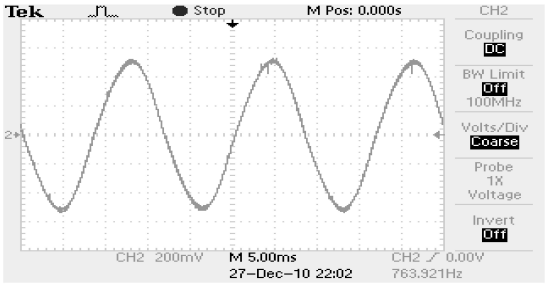
Figure 9. Experiement block diagram

Figure 12 displays the inverters fed from four separated dc sources. In this structure, the inverter can be corresponded to three-phase three-wire system; therefore, the output signals are obtained high-qualified performance at the load terminals without the third harmonic. In figure 13 laboratory measurements of phase voltages are shown when the inverter modulation is operated in different Vdc as well as modulation index m. The harmonic distortion (THD) for the output voltages is shown versus the increase in utilized fundamental frequency. This is because when the inverter is operated in lower frequency, times to charge and discharge

dc capacitors rise remarkably; as a result, the voltage ripple becomes more intolerable. More importantly, if the modulating frequency is exceeded the limitation of carrier frequency's sampling, harmonic content of output signals will be also magnified. In reality, some modulation in [4] are proposed to balance capacitor voltages by using redundant state selection RSS, or dc sources are derived from PV arrays to ensure the equivalent voltage supply for the inverter.







a) a-phase load current (simulation) b) a-phase load current (experiment)

Figure 10. Dual inverter experiement setup

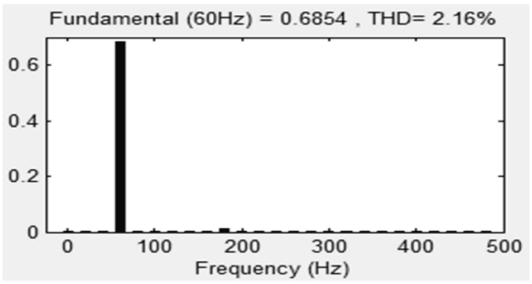
5.2. Experiments results with proposed techniques

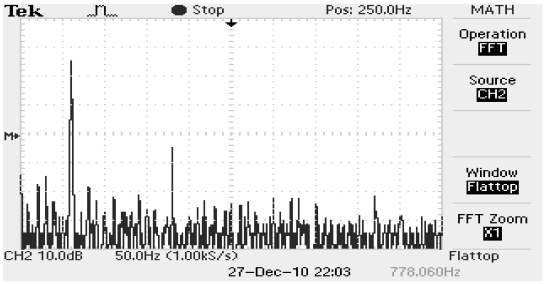
This experiment is realised with parameters $m = 0.8, fo = 50Hz, R = 16Ohms, L = 90mH, fs = 5kHz$

With the modulation applied, it can be seen in figure 14 that the even harmonic components of the output current are lessened considerably. Consequently, output signals are obtained by better harmonic performance.

6. CONCLUSIONS

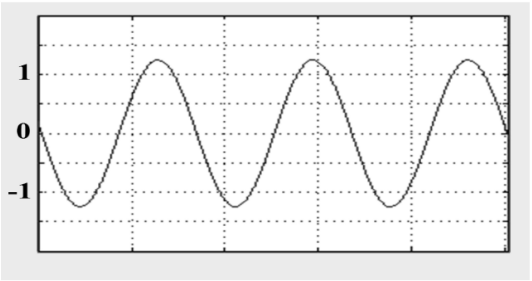
The novel carrier PWM algorithms of control for the cascade 3/3 diode-clamped inverter (wherein two three-phase three-level inverters connected in series through the load) have been

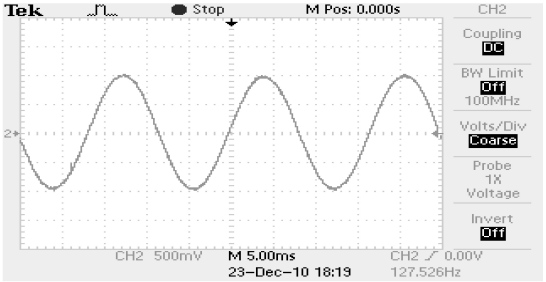




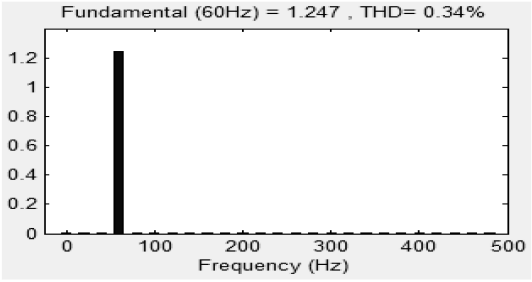
c) FFT analysis of current (simulation) d) FFT analysis of current (experiment)

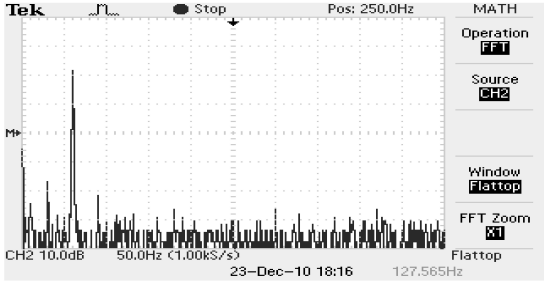
Figure 11. Simulation and experimental results when m = 0.4 and using only one dc source





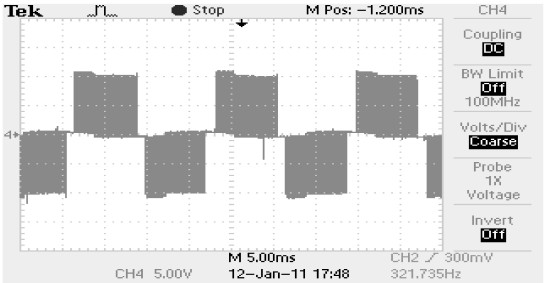
a) a-phase load current (simulation) b) a-phase load current (experiment)

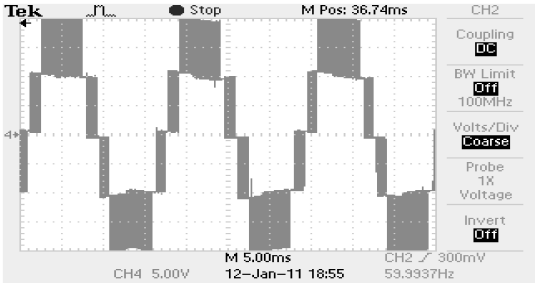




c) FFT analysis of current (simulation) d) FFT analysis of current (experiment)

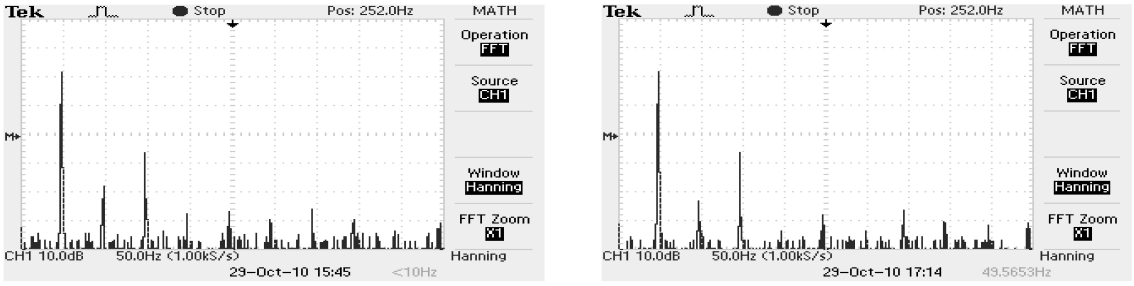
Figure 12. Simulation and experimental results when m = 0.8 and using 4 dc sources





a) Vdc =100V and m = 0.2 b) Vdc = 150V and m = 0.8

Figure 13. Experimental results of phase voltage



a)current's FFT (no proposed modulation) b)current's FFT (proposed modulation)

Figure 14. Comparison in output current's FFT

presented. Therein, the amplitude and frequency of output voltages can be produced symmetrically under the simultaneous change of three-phase references. Further advantages of the control methods are minimizing the voltage ripple, having the high power quality output with a lower THD, and operating the cascaded systems durably. Also, the topology in this paper can be supplied flexibly from the number of isolated voltage sources in distinctive applications such as in electric drive applications with a single voltage source used or in solar cell systems with independent DC sources. The experimental results all demonstrate the effectiveness of the proposed modulation methods.

REFERENCES

[1] H.Stemmler and P.Guggenbach, Configurations of High-Power Voltage Source Inverter Drives, *Proceedings of the European Power Electronics Conference* **1** (September 1993) 7–14.

[2] X. Kou, K.A. Corzine, M.W. Wielebski, Over-distention operation of cascaded multilevel inverters, *IEEE International Electric Machines and Drives Conference* **3** (June 2003) 1535–1542.

[3] S.Lu, K.A. Corzine, and T.H.Fikse, Advanced Control of Cascaded Multilevel Drives Based on P-Q Theory, *Proceedings of the IEEE international Electric Machines and Drives Conference* (May 2005).

[4] K.A. Corzine, M.W. Wielebski, F.Z. Peng, and J. Wang, Control of Cascaded Multi-Level Inverters, *IEEE Transactions on Power Electronics* **19** 3 (May 2004) 732–738.

[5] N.V.Nho,M.J. Youn, Comprehensive Study On SVPWM and Carrier Based PWM Correlation In Multilevel Inverters, *IEE-Proceedings Electric Power Applications* **153** 1 (Jan. 2006) 149–158.

[6] K.A. Corzine, S.D. Sudhoff, and C.A. Whicomb, Performance Characteristics of A Cascaded Two-Level Converter, *IEEE Transactions on Energy Conversion* **14** 3 (September 1999) 433–439.

[7] X. Kou, K.A. Corzine, M.W. Wielebski, Over-Distention Operation of Cascaded Multilevel Inverters, *IEEE International Electric Machines and Drives Conference* **3** (June 2003) 1535–1542.

[8] H.Stemmler, and P.Guggenbach, Configurations of High-Power Voltage Source Inverter Divers, *Proceedings of the European Conference on Power Electronics and Applications* **5** (September 1993) 7–14.

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